An Ultra-Low-Power Long Range Battery/Passive RFID Tag for UHF and Microwave Bands With a Current Consumption of 700 nA at 1.5 V

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***Abstract*—We present for the first time, a fully integrated battery powered RFID integrated circuit (IC) for operation at ultra-high frequency (UHF) and microwave bands. The battery powered RFID IC can also work as a passive RFID tag without a battery or when the battery has died (i.e., voltage has dropped below 1.3 V); this novel dual passive and battery operation allays one of the major drawbacks of currently available active tags, namely that the tag cannot be used once the battery has died. When powered by a battery, the current consumption is 700 nA at 1.5 V (400 nA if internal signals are not brought out on testpads). This ultra-low-power consumption permits the use of a very small capacity battery of 100 mA·hr for lifetimes exceeding ten years; as a result a battery tag that is very close to a passive tag both in form factor and cost is made possible. The chip is built on a 1-μm digital CMOS process with dual poly layers, EEPROM and Schottky diodes. The RF threshold power at 2.45 GHz is -19 dBm which is the lowest ever reported threshold power for RFID tags and has a range exceeding 3.5 m under FCC unlicensed operation at the 2.4-GHz microwave band. The low threshold is achieved with architectural choices and low-power circuit design techniques. At 915 MHz, based on the experimentally measured tag impedance (92-j837) and the threshold spec of the tag (200 mV), the theoretical minimum range is 24 m. The tag initially is in a "low-power" mode to conserve power and when issued the appropriate command, it operates in "full-power" mode. The chip has on-chip voltage regulators, clock and data recovery circuits, EEPROM and a digital state machine that implements the ISO 18000-4 B protocol in the "full-power" mode. We provide detailed explanation of the clock recovery circuits and the implementation of the binary sort algorithm, which includes a pseudorandom number generator. Other than the antenna board and a battery, no external components are used.**

***Index Terms*—18000–4B, active, battery, International Standards Organization (ISO), microwave, passive, RFID, Schottky diode, tag, ultra-high frequency (UHF), ultra-low power.**

I. Introduction

THERE has been an exponential growth in RFID deployment for various industries such as automated toll collection for bridges, automated data collection and tracking of articles on conveyor belts, anti-theft protection for high value merchandise and automatic billing at point of sale counters. One of the main advantages of RFID is the ability to communicate at a distance—this nonproximity based reading of transponders will make RFID the "next generation bar code" if the cost of the tag can be brought down. Nonproximity based reading also enables RFID tags to be used as access cards (for identification to enter into a restricted area), contact-less sensors (for pressure, temperature) etc.

As of today, RFID tags operate in several bands—high-frequency (HF) (13.56 MHz), ultra-high-frequency (UHF) (860–915 MHz), and microwave bands (2.4 GHz). Transponders that operate at 125 kHz [1] and 13.56 MHz [2] have been widely deployed for a number of years. The main disadvantage of them is limited range typically (less than 2 m). Passive transponders that operate in the UHF band have ranges of 7.5–9 m [3], [4], and transponders that operate in the microwave band have ranges under 2 m. Karthaus *et al.* [4] reports a low-power RFID chip for UHF with very low power consumption which is obtained by the combination of pulsewidth modulation on the forward link (base-station to tag) with low RF-off times (no excess voltage droop on the on-chip power capacitor) and phase-shift keying (PSK) on the return link (tag to base-station) greatly facilitates working of the tag at large ranges. A high level description of a passive RFID chip that implements the EPC Class 0 protocol is provided in Glidden *et al.* [5]. De Vita *et al.* [6] provides a design criteria for the front-end of passive RFID tags. Nakamoto *et al.* details an RFID tag using ferroelectric memory [7]. Much work has been done on using CMOS front-ends and CMOS technology for RFID [8]–[12].

While the range for passive RFID tags at UHF and microwave is adequate for many applications, there are applications that require greater range. For greater range, an active transponder is required. The disadvantage of an active transponder is that it requires a battery and as a result the transponder will have a finite lifetime. Furthermore the battery should have a small form factor so that it can be seamlessly used in the assembly process for large volume production. The requirement of long lifetimes (usually in excess of 10 years) and the small form factor necessitates a battery of very small capacity- this translates to low power consumption on the active transponder for it to work throughout the full life of the tag.

This paper presents an ultra-low-power active tag that has a lifetime in excess of 10 years with a tiny 100-mA·h battery (for comparison an AA battery capacity is 2100 mA·h). The long lifetime of the battery tag makes it highly attractive for applications where a large range is required while at the same time adding very little cost from the use of a small battery. Furthermore when the battery dies, the tag will continue to work as a

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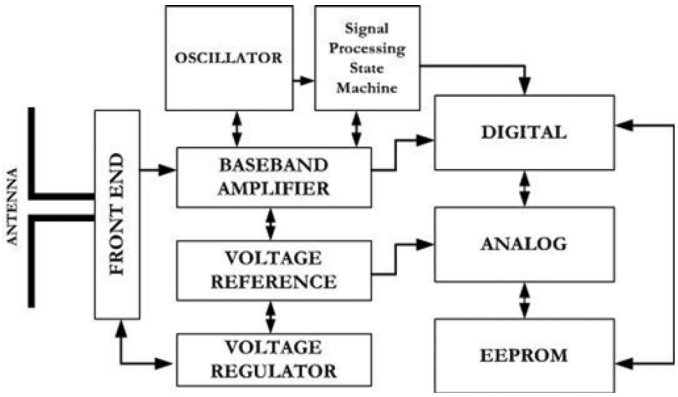

Fig. 1. Block diagram of the whole chip.

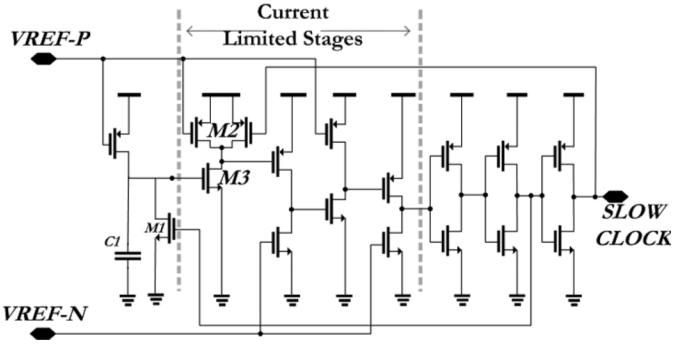

Fig. 2. Low-power oscillator that clocks the chip when it is in the "low-power" mode.

passive tag [13]. This novel feature overcomes one of the major drawbacks of currently available active tags namely that the tag cannot be used once the battery runs out and data stored on the tag is lost forever.

II. Architecture

A passive low-power tag typically has a power consumption of a few microamps [1] while it is communicating with a base station. An operating current of a few micro-amps is a significant source of power drain especially with a low-capacity battery and time periods exceeding ten years. Most of the time, the tag is sitting in a standby mode (where it does not receive or transmit commands); lesser the power consumed in the standby mode, greater is the lifetime of the tag. For this reason we architected the tag to work in a "low-power" mode and "full-power" mode. In the "low-power" mode, most of the tag circuitry is shut down and thus power dissipation is brought down to a minimum but the range of the tag is unaffected. In the "low-power" mode the tag is constantly looking out for a command that will put it into the "full-power" mode. Once the tag is in the "full-power" mode, all tag circuits are fully functional and current consumption increases as a result; in this mode the transponder accepts and executes commands specified in the ISO-180004B [14] protocol for operation in the Microwave band. The tag will go back to the "low-power" mode if it does not detect any data for a period of 100 ms (the typical period of time during which the base station transmits RF power at a particular frequency from a set of pseudorandomly selected frequencies). A simple command is used to put the tag back into the "full-power" mode from the "low-power" mode, which is the bit sequence "1001" at a data-rate of 2.5 kHz (different from the nominal data-rate of 32 kHz). The "full power" command detection module consists of a current controlled oscillator, a front-end block that rectifies the signal from the base station, a baseband comparator, and a signal processing state machine that decodes the incoming pattern (Fig. 1). These four circuits are required to function at very low power. As a result any complex filtering/decoding algorithms were ruled out. Detailed description of these various blocks are provided in Section III. Fig. 1 shows a high-level block diagram of the entire chip.

The tag also has on-chip EEPROM (1 k), clock recovery and demodulation circuitry and control logic that implement the ISO-18000–4B protocol [14]. We provide detailed discussion and schematics of the "full-power" detection module and also the analog blocks that are crucial to implementing the ISO-4B protocol which includes clock recovery circuits, voltage regulation and implementation of the binary sort algorithm.

III. Building Blocks

A. Low-Power Oscillator

Fig. 2 shows the circuit schematic for the low-power oscillator. This circuit uses voltage reference signals VREFN and VREFP which generate constant current on a unit sized (5/10) nMOS and pMOS transistor, respectively. The circuit works as a ring oscillator with seven inverter stages; four of these stages (after transistor M2) as shown in Fig. 2 have current limited loads (transistors that are driven by reference voltages VREFN and VREFP; these operate in subthreshold saturation and source/sink constant current) and the delay across the four stages determines the pulsewidth of the oscillator output. The minimum pulsewidth (which is equal to the duration of two voltage-rise transitions and two voltage-fall transitions on the current-limited stages) is chosen to provide adequate hold-time for the flip-flops that are clocked by the low-power oscillator. When the output signal SLOWCLOCK is low, transistors M1 and M2 are turned on; M1 discharges the voltage on *C1* thereby turning off M3; and M2 quickly charges the drain of M3 to a high. This toggles the output voltage at SLOWCLOCK and SLOWCLOCK goes high; M2 and M1 are turned off and capacitor *C1* is slowly charged. When the voltage on *C1* becomes high enough to turn on M3, output voltage at SLOWCLOCK is toggled. The time to charge *C1* determines the frequency of the oscillator. The frequency of the oscillator could vary by as much as $\pm 20\%$ owing to process variations; the restriction of low power prevents the usage of any frequency correction schemes. The frequency variation is compensated for in the signal processing state machine and is explained in Section III-E of this paper.

B. Front-End and Voltage Regulation

Fig. 3 shows RF front-end and voltage regulation stage of the transponder. The transponder decodes amplitude-shift keying (ASK) signals from base station. The front-end consists of a Schottky diode based voltage doubler circuit that provides a high-Q both at UHF and microwave bands. The front-end is connected to a matched antenna to capture RF power transmitted from the base station. The rectified RF envelope is stored on capacitor *C1*. In Fig. 3 RETURN_LINK is high when the tag is

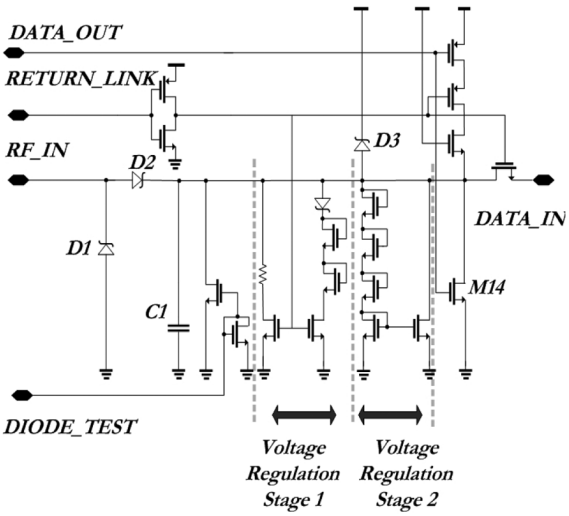

Fig. 3. RF front-end on the chip with the voltage regulators and the modulator for back-scattering.

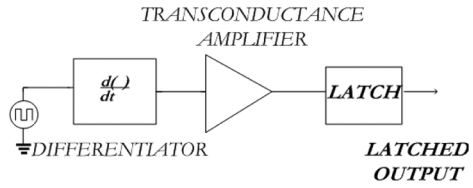

Fig. 4. Baseband amplifier architecture.

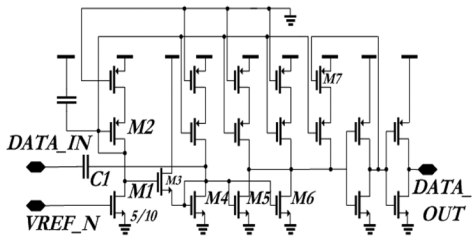

Fig. 5. Baseband amplifier circuit schematic.

sending data back to the base station. We architected the voltage regulation on the chip in two stages. "Voltage regulation stage 1" is only active when the tag is not sending data back to the base station and provides a discharge path for charge stored on the capacitor *C1* as well as a nominal voltage clamping action—this will ensure that *C1* can track the incoming RF envelope. This first stage is primarily functioning when the voltage on the chip is less than 3.6 V and can also sink a limited amount of current and it primarily operates in the far-field(of the base-station antenna). "Voltage regulation stage 2" consists of a diode stack with a driver and primarily operates when the voltage on the chip exceeds 3.6 V; this stage can sink a large of amount of current and is primarily functioning when the tag is in the near field, where it prevents a large voltage from building up on the chip. By drawing a large current it simultaneously detunes the front-end, resulting in less power absorbed. Thus, the voltage clamping action of the regulator is two fold—firstly it raises the power consumption on the chip thereby preventing the on-chip voltage from building up and secondly it detunes the front-end, further preventing the voltage from building up. Experimental measurements relating to the voltage regulator are presented in Section V-A. DATA_OUT is digital data that the tag is sending back to the reader and it drives a modulator transistor M14 that modulates the impedance that is seen from the antenna and thereby provides a ASK back scatter signal to the base station. Also note that diode D3 that connects the rectified RF signal to supply bus; when the battery is active, diode D3 is reverse biased; however when the battery is dead, D3 provides power to the tag from the rectified RF signal. Thus, the tag operates as a battery tag when the battery has sufficient charge and as a passive tag when the battery is dead. There is another diode that is connected between the battery and the supply bus (not shown) so that the battery does not short the supply bus when it dies. The output DATA_IN of the front-end block is supplied to the base band amplifier.

C. Baseband Amplifier

We examine the constraints on the amplifier circuit that were necessary on this chip, analyze the architecture that we selected, and finally present the circuit schematic.

The amplifier is required to have very low power consumption—the current drawn must be less than 120 nA throughout the entire life of the battery as well as during passive mode of operation of the tag. The amplifier must capture signals with 100% modulation as well as fractionally modulated signals (the input common mode voltage can vary from ground to near the supply voltage). Because of the wide range of the modulation index, the amplifier must have a large dynamic range for decoding ones and zeroes. Finally, the amplifier must not be sensitive to stray noise signals that are lower in amplitude than the minimum required input signal or to high frequency signals that have greater data-rates than what is permitted (this restriction is there to prevent the tag from staying indefinitely in the "full-power" mode). To summarize, the constraints on the base-band amplifier are ultra-low-power consumption (less than 120 nA), ability to decode variable indexes of modulation (varying from 10% to 100%), and immunity to stray noise in the RF environment.

The architecture we selected for implementation is shown in Fig. 4. The input stage consists of a differentiator, followed by an amplifier and finally a latch stage for storing data indefinitely. The circuit schematic is shown in Fig. 5. The differentiator consists of capacitor *C1* connected to diode-connected transistor M4 (which provides a low-impedance node); M4, M5 and M6 constitute the amplifier and M7 constitutes the output latch. When a square wave voltage is present at the input of capacitor *C1*, there is a positive voltage spike (differentiation operation) at the drain of M4 for a rising data transition and a negative spike at the drain of M4 for a falling data transition. This trips the amplifier stage with transistors M5 and M6. Amplifier stages with M4, M5 and M6 are biased by current sources of the same value so that when the output DATA_OUT is low, M7 is turned off and the drain of M5/ M6 is low (the channel lengths for M5/M6 are smaller than that for M4). When DATA_OUT is high, M7 is turned on and the drain of M5/M6 is high. In order for M5/M6 drain voltage to change in magnitude from high to low the input signal should be of enough strength to cause M5/M6 to sink 3 unit current sources and let the drain of M5/M6 turn low. And for M5/M6 drain voltage to go from low

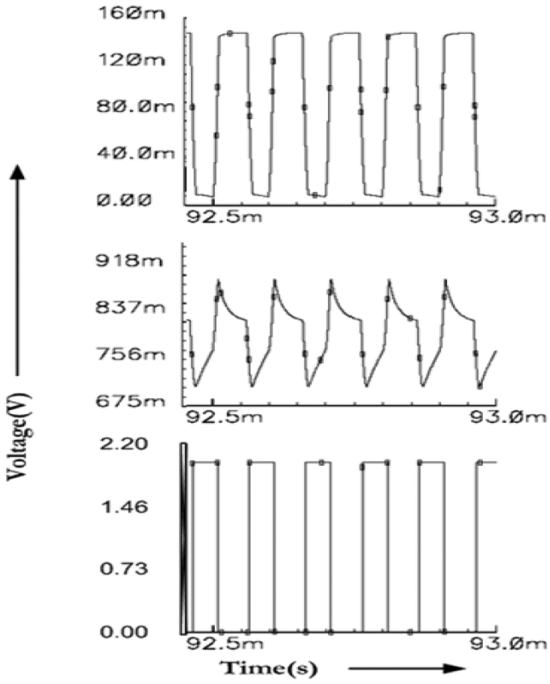

Fig. 6. Simulation results of the baseband amplifier. From top to bottom (a) Input square wave going into the baseband amplifier at node. (b) The differentiated signal at capacitor *C1*. (c) Output of the baseband amplifier.

to high, the input signal should be of enough strength to cause M5/M6 to turn off and permit its drain voltage to rise. For input signals that do not do either of these, the amplifier is insensitive and its current output state is maintained. M7 serves as a latch that maintains the current output state following a transition at the drain of M5/M6. Fig. 6 shows the simulated voltages (simulations were done with Cadence Spectre circuit simulator) at various nodes: 1) the input signal waveform; 2) the differentiated signal at capacitor *C1*; 3) latched output. The amplifier does not respond to signals that have data-rate exceeding 300 kHz and therefore the tag is unaffected by other interfering signals with data-rates exceeding 1 MHz and which operate in the same band.

Thus, we use a very simple architecture, without any complicated filtering/biasing schemes to achieve all the rigorous constraints on the amplifier listed at the beginning of this section. The same architecture can be used to lower the threshold of the amplifier even more by increasing the bias current in the amplifier. The lower threshold will provide greater range for the tag but will lower the lifetime of the tag for a given battery capacity.

D. Reference Generation

In this section we examine the primary requirements for the bandgap/startup circuit and reset signal and provide detailed explanations for the circuit schematic. In the active mode of operation, the tag will be powered by a battery till the battery dies out, after which it will function as a passive tag. A one-time reset (RESET) is to be provided to all circuits on the chip when a battery is attached for the first time. Furthermore when the battery dies out and the tag works as a passive tag, this reset signal should go active when the supply voltage falls below 1.3 V (to prevent data corruption in the EEPROM). The constraints on the startup circuit are as follows: 1) the circuit should be active even for supply voltages less than 1 V(when the on-chip voltage drops down); 2) the circuit must continue to function when the on-chip voltage stays indefinitely at a voltage less than 1 V (in other words, a timing circuit which turns off after a certain time cannot be used)—this scenario occurs when the tag is at a weak field region/fringe field, where it is powered and un-powered randomly; 3) the circuit cannot draw any steady state current as even a small current would be a prohibitive drain on the available power over the tag lifetime. Fig. 7 shows the reference generating block. A CMOS "bandgap" circuit [15] is used for reference voltage generation. The start-up circuit sinks current into he drain of M18 if its drain voltage is at ground. M7 acts as a large resistor; when the supply voltage builds up to more than 1.3 V, the drain of M7 is gradually charged and turns it off; when M7 drain is being charged, M8 sinks current into the drain of M18 to bring it out of the 0 bias state. This is illustrated in Fig. 8 with transistor M7 represented as a resistor. When the supply voltage build up very slowly (as when the tag is in a region of weak field), and the on-chip voltage is less than 1.3 V, M6 starts to conduct and keeps the drain of M7 at ground. M6 is turned off only when the supply voltage is greater than 1.3 V (explained below). This is illustrated in

Fig. 9 with transistor M7 represented as a resistor. Inverter stage with transistor M4 works as a level detector circuit. When the supply voltage is less than 1.3 V, the output of this stage is a high, and it is used to turn on the reset signal as well as the start-up circuit (as explained in the previous paragraph). When the supply voltage is greater than 1.3 V, the output stays low. M16, M17 and capacitor *C3* comprise the reset generation block. At power-up, capacitor *C3* is uncharged and the output RESET is high (this resets all circuits on the chip); *C3* is gradually charged by M16 setting RESET to low. When supply voltage goes below 1.3 V, M17 is turned on and discharges *C3*, setting RESET high again

1) Clock Recovery Block: In this section, we describe the clock recovery mechanism for the tag. Clock recovery is done only when the tag is in the "full-power" mode. The on-chip clock is determined by the data-rate on the forward link (reader to tag communication). The chip must be able to lock on the datarate of modulation from the base station and conform to this data-rate when it communicates with the base-station. The clock recovery unit uses a successive approximation register (SAR) based algorithm to capture the data rate. The successive weights (which are current sources) are controlled by the digital section and their setting is based on the header preamble of the incoming command. We first describe the method of calibration of the oscillator which is in part mandated by the protocol (refer to Section III-E-II) and by the chip architecture (refer to Section III-E-III).

2) Calibration: The calibration of the chip is enabled on the receipt of a valid command. The header of every command according to the ISO18000–4 B protocol has an 8 bit preamble consisting of Manchester '0' bits (Fig. 10). The start of the calibration cycle is enabled by the digital section of the chip. During each bit of the preamble, each one of the control bits from SAR4 to SAR0 is set, so that at the end of the calibration cycle, the frequency control bits are all set to the data-rate of the reader.

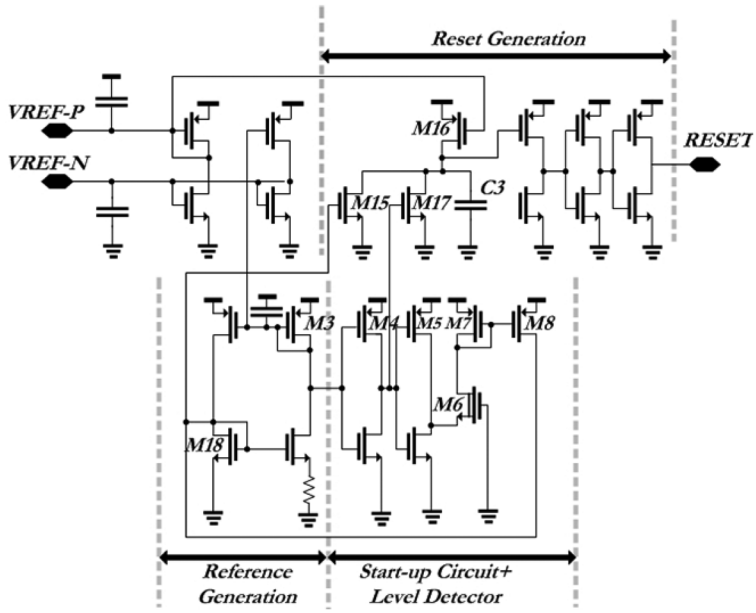

Fig. 7. Voltage reference, start-up circuit, and reset generation.

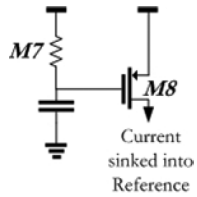

Fig. 8. Equivalent circuit for start-up circuit at power-up.

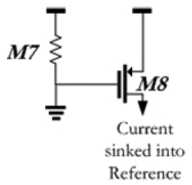

Fig. 9. Equivalent circuit for start-up circuit when the supply voltage is less than 1.3 V.

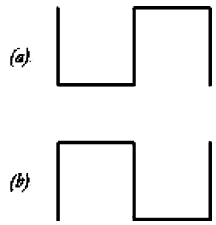

Fig. 10. (a) Manchester "0" bit. (b) Manchester "1" bit.

At the end of the calibration cycle, signal CAL_DONE is activated and this slows down the oscillator; the primary reason for slowing down the oscillator is to correct for errors in calibration. There is a finite amount of pulsewidth distortion present on the forward link; this pulsewidth distortion is not taken into account during the preamble phase as the bit boundaries are defined from one rising edge to another rising edge. But while decoding data which can commence from a rising edge to a falling edge, it is important to take into account the inherent pulsewidth distortion in the chip front-end. Thus, the slowing down of the oscillator takes care of pulse-width distortion in the data stream as well as errors in calibration.

3) Clock Recovery Architecture: The SAR based oscillator sets its frequency based on whichever of the SAR bits (SAR4 to SAR0) are turned on. The calibration cycle is 6 bits long and takes place during the preamble of an incoming command. Each of the binary weights contribute to the final frequency in a binary weighted manner. SAR4 has the highest weight and when it alone is turned on, the chip runs at half of the highest frequency; SAR3 when turned on alone, makes the chip run at one-quarter of the highest frequency and each of the remaining bits sets the chip frequency at ½ of the previous bit. Each of the binary weights control a current source (the current value being proportional to the weighting bits contribution to the frequency; e.g.,- the current controlled by SAR3 is one-half of the current controlled by SAR4). The current contributed by each bit is summed to a summing node with capacitor *C2* in Fig. 11. During the first 6 bits of the preamble, the SAR register setting is adjusted as shown in Fig. 12. Top half of Fig. 12 shows the modulated waveform from the basestation; the first rising edge to the second rising edge transition, the oscillator runs with the SAR setting of 10000 (only the highest weight is turned on). The output of the oscillator is counted with a pulse counter in the digital section; at the second rising edge data transition, if the number of pulses counted is less than 8 then the SAR4 is left turned on and during the second rising edge to rising edge transition, the SAR setting is 11000. At the end of the third rising edge data transition, if the number of pulses counted is less than 8, then SAR3 is left turned on. In this manner all of the SAR bits are sequentially turned on/off so that at the end of the calibration cycle, the output of the oscillator is very close to 8x times the baseband modulation frequency of the incoming RF signal.

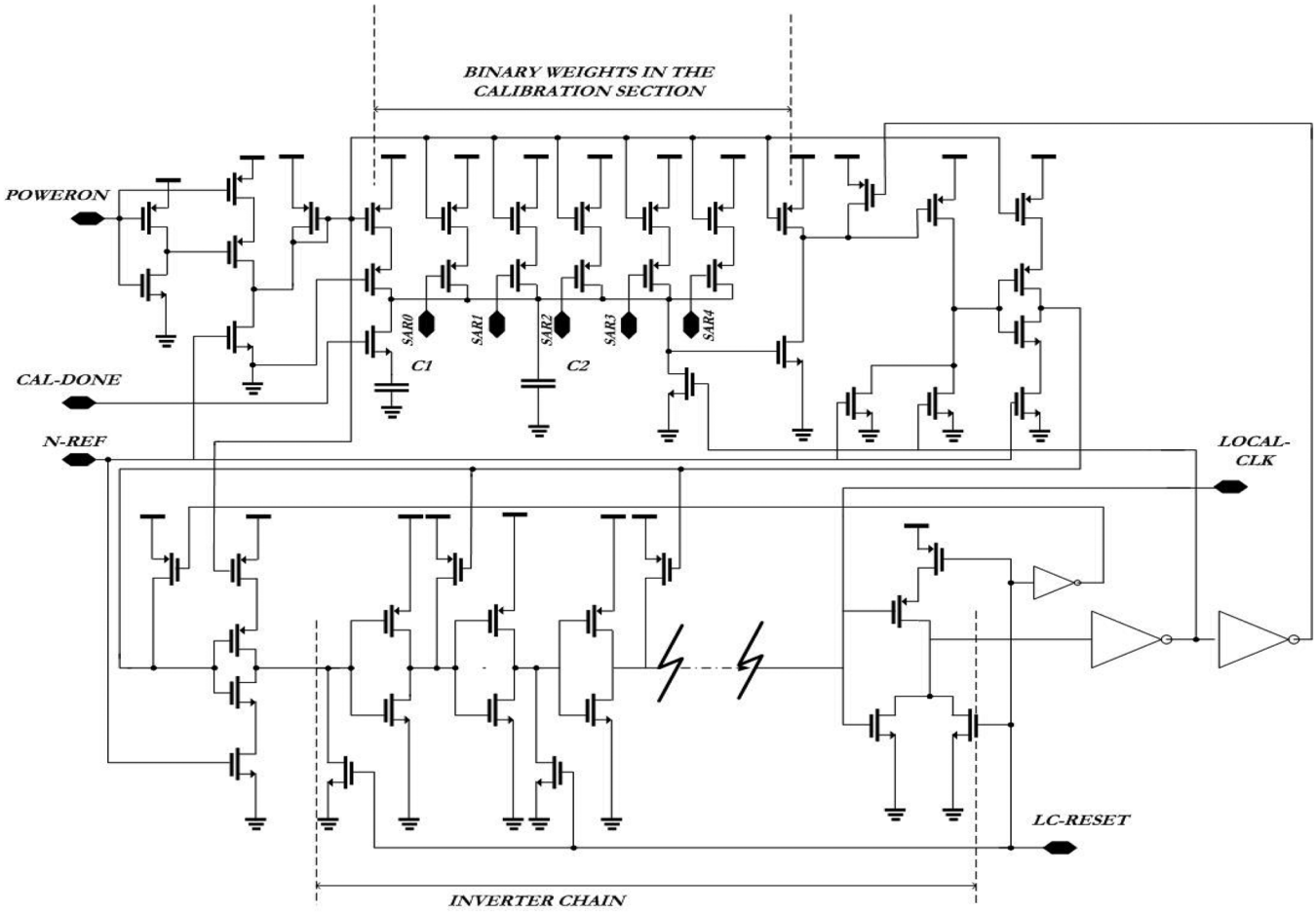

Fig. 11. Circuit schematic of the current controlled oscillator.

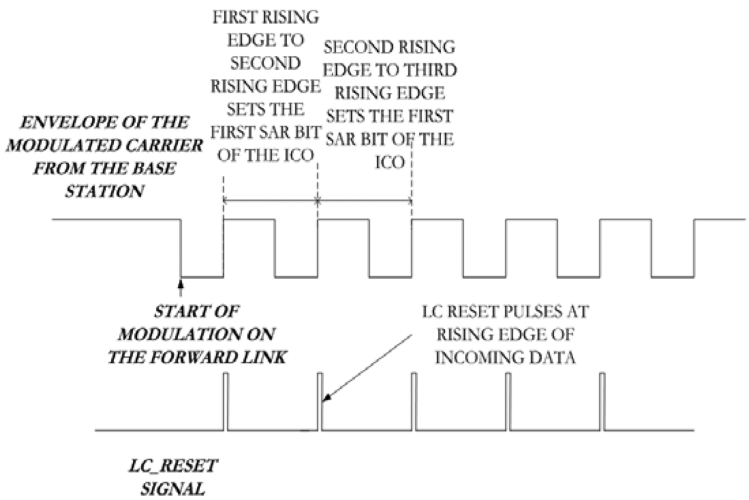

Fig. 12. Calibration of the clock recovery block to the incoming command from the base station. The lower figure shows the generation of the *LC*_RESET signal that is used to reset the phase of the oscillator as well as to reset the digital section to the next round of calibration.

The delay of the inverter chain (bottom of Fig. 11) determines the pulsewidth of the oscillator output. The binary weights in the calibration section (top of Fig. 11) are current sources that supply current onto the summing capacitor *C2*. A factor of 2 is used in scaling, this means that if SAR1 supplies a current of I, then SAR2 supplies a current of 2.I, SAR3 supplies a current of 4.I; the scaling of currents is done by reduction of the widths of the transistors. At the end of calibration, signal CAL_DONE (in Fig. 11) goes high and adds another capacitor *C1* in parallel to the summing capacitor *C2*. This slows down the ICO by a factor depending on the relative sizes of *C1* and *C2* and is done to adjust for errors in calibration and also to account for pulsewidth distortion. Another input to the oscillator is *LC*_RESET, which is a narrow pulse occurring at the rising edge of data; this provides a reset signal to the digital section to initiate the next step in the calibration cycle (as described above). *LC*_RESET is also

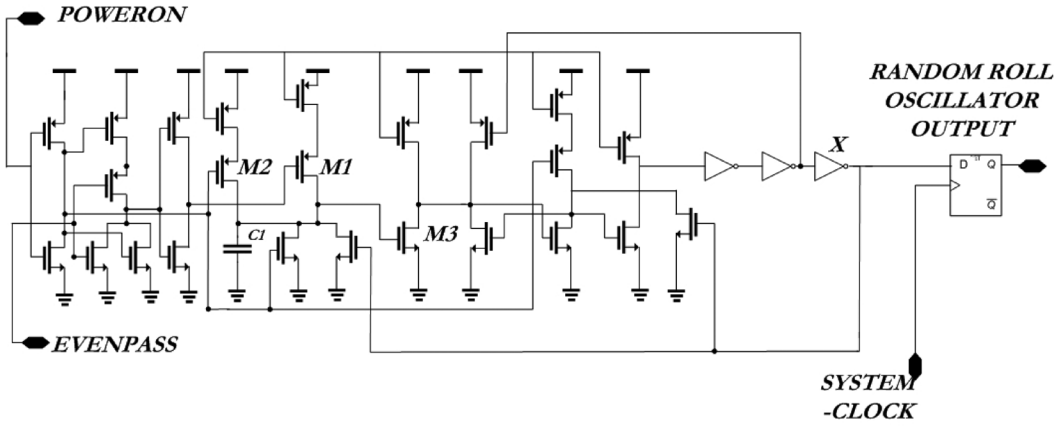

Fig. 13. Circuit schematic for the random roll oscillator which is used for generating random bits for the binary sort algorithm.

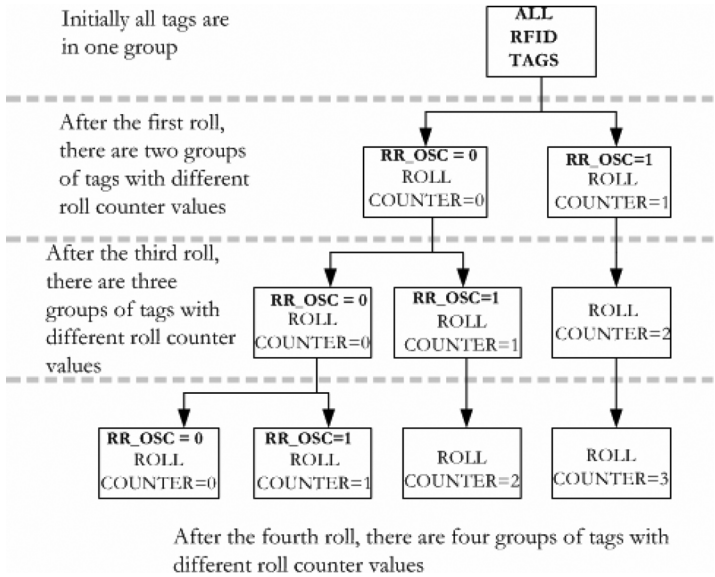

Fig. 14. Illustration of the binary sort algorithm.

provided to the inputs of clamping transistors within the ICO; this ensures that a stray pulse that was propagating down the inverter chain (and coincident with an incoming rising data transition) will not be falsely counted as a pulse during the next rising edge to rising edge period.

4) Random Roll Oscillator: The random roll oscillator is primarily used for the binary sort algorithm for singulating a tag (refer to Section III-G). This requires an oscillator that exhibits considerable variation from one chip to another chip, in other words the frequency of the oscillator is made to depend as much as possible on process variations. The basic architecture of the random roll oscillator is that of a ring oscillator with each stage of the ring oscillator current limited (to reduce power consumption). Fig. 13 shows the circuit schematic for the random roll oscillator. The oscillator is turned on only when signal POWERON is active (after the tag is in the "full-power" state). The charging of capacitor *C1* determines the period of the oscillator. Capacitor *C1* turns off transistor M3 as it is charged to the threshold voltage of M3. In order to maximize the variability of the oscillator, transistor M3 is made of the smallest length possible. The output of the oscillator (point X in Fig. 13) is then sampled with the system clock (which is based on the modulation frequency of the incoming RF signal) to generate the random roll output. In order to provide even more variability, the frequency of the random roll oscillator is dithered by EVEN_PASS. EVEN_PASS is generated by the digital section of the chip and is based off the unique ID of the chip and the state of the tag during tag singulation. When EVEN_PASS is turned on, the gate of M1 is high and turns off M1, resulting in a smaller charging current for capacitor *C1*, which increases the period of oscillation. The frequency variability introduced by the intentional design of the oscillator and the dither control using signal EVEN_PASS gives a reasonably random output signal for the oscillator.

5) Binary Sort Algorithm and Tag Singulation: The battery tag executes the ISO18000-4B protocol and performs tag singulation in the manner as mandated by the protocol. The tag singulation uses a binary sort algorithm. The algorithm is as shown in Fig. 14. At the beginning all tags are in one group and a command is issued to all tags to roll a random number. Those that roll a random number value of 0 will have a counter value of 0 and those that roll a random number value of 1 will have a counter value of 1. Only those tags that have a counter value of 0 will respond to the base station command; tags with a nonzero

counter value remain quiet. If there is still more than one tag with a counter value of 0, then the base station issues another command to all tags to roll another random number. All tags that have a nonzero counter value will not roll a random number and will only increase their counter value by 1. In this manner, the base station issues commands to the tags until there is only a single tag with a counter value of 0, whose ID is then extracted. Now there are different classes of tags each having a different value of the roll counter. When there are no more tags with a counter value of 0, the base station will issue a command to all tags to reduce their counter value with the result that all tags that formerly had a counter value of 1, will now have a counter value of 0. Again the base station will issue commands to ensure that one tag alone remains with a roll counter of 0. Very critical to the binary sort algorithm is that the random number generated by tags with a roll counter of 0 is sufficiently random. Otherwise it will result in considerable latency and protocol overhead in tag identification. As described in Section III-F-I, the random roll oscillator produces an output that is made to vary as much as possible with process variations and additional frequency dither is introduced with the EVEN_PASS signal; the output of the random roll is then sampled by the system clock (which is recovered from the command issued by the base station), to generate a random sequence

E. Signal Processing State Machine

The signal processing state machine is clocked by the low-power oscillator. The chip has two modes of operation- "full-power" mode and "low-power" mode. In the "low-power" mode most of the tag circuitry (that decode ISO18000-4 B commands) is shut down to save battery power. The chip comes out of the "low-power" mode into the "full-power" mode only after it detects a valid "full-power" command. The "full-power" command consists of "1001" pattern with each bit lasting for 400 us—the intent was to use a simple pattern that is nonrepetitive to make the decode circuitry as simple as possible as well as to avoid interference with other tags (the data-rate for the "full-power" command is significantly different from the normal tag communication data-rate, thus minimizing interference). After a field low is detected, the state machine starts looking out for the full power command; the duration(in terms of oscillator counts) of the header "1" bit of the pattern is used as a reference to check the duration of the next two "0" bits; if the duration of the two "0" bits is twice the duration of the initial "1" bit, then on receiving the next valid "1" bit the state machine flags a power-up signal to the rest of the chip. The power-up signal enables rest of the tag circuitry to start decoding valid commands from the incoming rectified RF envelope and sending data back to the base station. If no further data transitions are detected for 100 ms, the tag goes back into the "low-power" mode and keeps looking for the next "full-power" command. The state machine also rejects data that is out of band from the expected data range. Fig. 15 shows a flowchart of the algorithm implemented by the state machine. Fig. 16 shows the variation of the oscillator frequency (slow and fast) due to process variations. Since the oscillator is driven by a constant current source charging a capacitor, process variations could shift the frequency by as much as $\pm 20\%$. This means that the number of samples taken during each bit period of the "full-power" command would show a corresponding variation but the state machine allows for this variation. Since both the incoming pattern and the oscillator are asynchronous, so depending on the phase offset between the oscillator and the "full-power" command, the number of sample points for each successive bit could be off by 1 and hence there is no fixed ratio (in terms of number of samples) for successive bits in the "full-power" command. Taking into account all possible scenarios, there is a possibility of the tag awakening on a false pattern; but in this case the tag will go back to the low-power mode if no data transitions are detected for 100 ms.

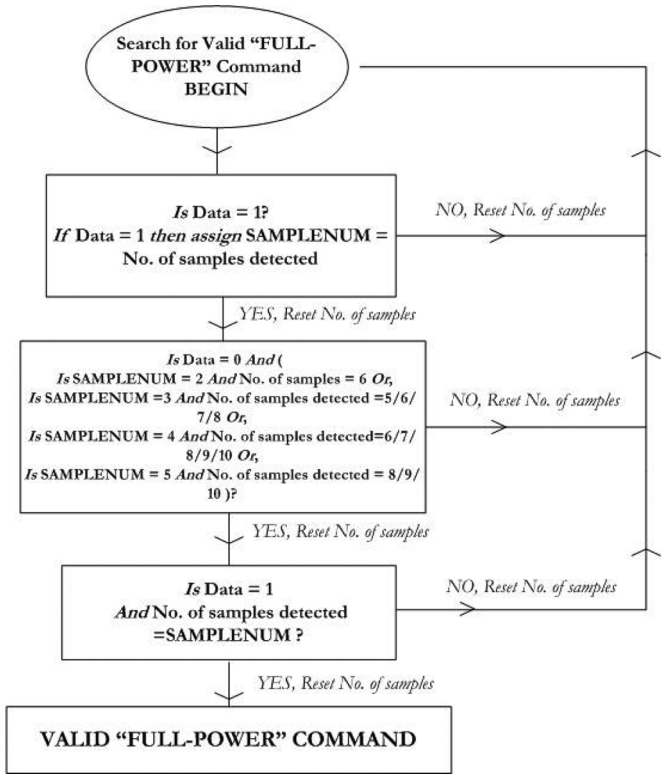

Fig. 15. Algorithm implemented by the signal processing state machine. SAMPLENUM is the number of samples detected during the first bit period, data is sampled incoming data and the number of samples is reset at every block transition.

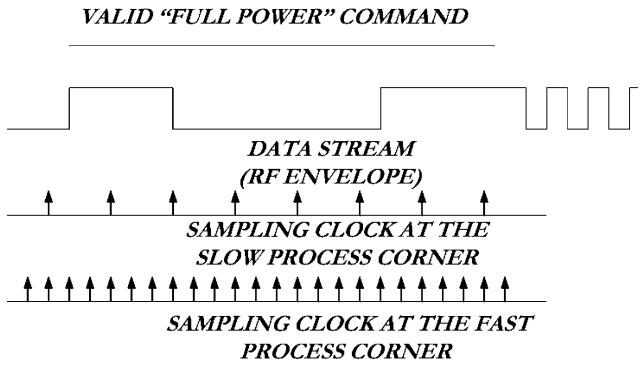

Fig. 16. Sampling of incoming command when the oscillator runs slow and when the oscillator runs fast.

A micrograph of the chip is shown in Fig. 17 (which has an area of approx. 2 mm $\times$ 2.5 mm) and a prototype tag with the chip wire-bonded to the antenna traces and globbed, with battery attached is shown in Fig. 18.

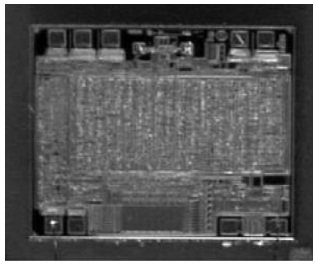

Fig. 17. Micrograph of the chip.

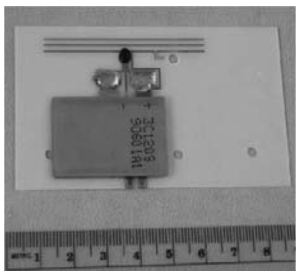

Fig. 18. Photograph of the assembled tag (chip wire-bonded and globbed to FR404 substrate) with a thin battery attached.

IV. Tag Read Range

In this section we derive the range of the chip as a function of chip impedance and the base-station transmit power. The RF power transmitted by the base-station is termed emitted isotropic radiated power (EIRP)—this is the sum of the RF output power and the gain of the antenna. At a distance R_r from the base-station antenna, the receive power density is given by

$$P_{\text{rec}} = \frac{\text{EIRP}}{4 \cdot \pi \cdot R_r^2}. \tag{1}$$

Using the Friis transmission equation, the incident power on a tag antenna of gain G_{tag} and at a distance R_r from the base-station antenna is given by

$$P_{\text{tag}} = \frac{\text{EIRP} \cdot G_{\text{tag}} \cdot \lambda^2}{16 \cdot \pi^2 \cdot R_r^2}. \tag{2}$$

If we assume an antenna (with impedance $R_a + jX_a$) that is conjugate matched to the chip (with impedance $Z_{\text{chip}} = R_{\text{chip}} + jX_{\text{chip}} = R_a - jX_a$) then the total power absorbed by the combination of chip and antenna is

$$P_{\text{abs}} = \frac{V_{\text{RF}}^2}{4 \cdot R_{\text{chip}}} \tag{3}$$

where V_{RF} is the peak RF source voltage. The RF voltage at the input of the chip is given by

$$V_{\text{chip}} = \frac{V_{\text{RF}} \cdot |Z_{\text{chip}}|}{2 \cdot R_{\text{chip}}}. \tag{4}$$

Since the front-end is a voltage doubler, the dc voltage developed on the chip is given by

$$V_{\text{dc}} = 2 \cdot (V_{\text{chip}} - V_{\text{Schottky}}) \tag{5}$$

where V_{Schottky} is the Schottky diode turn-on voltage. Expressing the dc voltage on the chip in terms of the source RF voltage (V_{RF}) and neglecting the Schottky diode drop, and noting that the far-end of the range of the tag is reached when the dc voltage on the chip equals the minimum dc threshold voltage on the chip $(= V_{\text{th}})$, the relationship between the range of the tag, the threshold voltage and the chip impedance can be found, as shown in (6), at the bottom of the page, where

R_r	range of the tag ;
λ	wavelength of operation ;
EIRP	power radiated out by the base-station (4 W) ;
Z_{chip}	impedance of the chip ;
G_{tag}	gain of the tag(2.15 dB for a dipole);
R_r	range of the tag ;
V_{th}	dc threshold voltage at which the chip can decode a command(0.2 V);
τ	impedance match factor $(= 1)$;
V_{Schottky}	Schottky diode turn-on voltage.

One can easily see that in order to maximize the tag range(provided the antenna is matched to the chip, i.e., $\tau = 1$), the reactance of the chip must be maximized, whereas the resistance and the threshold voltage must be minimized.

V. Experimental Results

A. Chip Characterization

Fig. 19 shows a command issued to the chip at a baseband frequency of 32 kHz; the baseband command simulates a command issued to the tag in the field without the carrier. The amplitude of the baseband command is 360 mV and with a 0.2 V Schottky diode drop, the signal reaching the baseband amplifier is 160 mV; the response of the chip to the command is also shown in the Fig. 20 (when the tag is in the field this signal would modulate the front-end, backscattering the data back to

$$R_r = \lambda \cdot \sqrt{\tau \cdot \left[\frac{G_{\text{tag}} \cdot \text{EIRP}}{16 \cdot \pi^2}\right] \cdot \frac{\left|Z_{\text{chip}}^2\right|}{R_{\text{chip}}} \cdot \left[\frac{1}{(0.5V_{\text{th}} + V_{\text{Schottky}})^2}\right]} \tag{6}$$

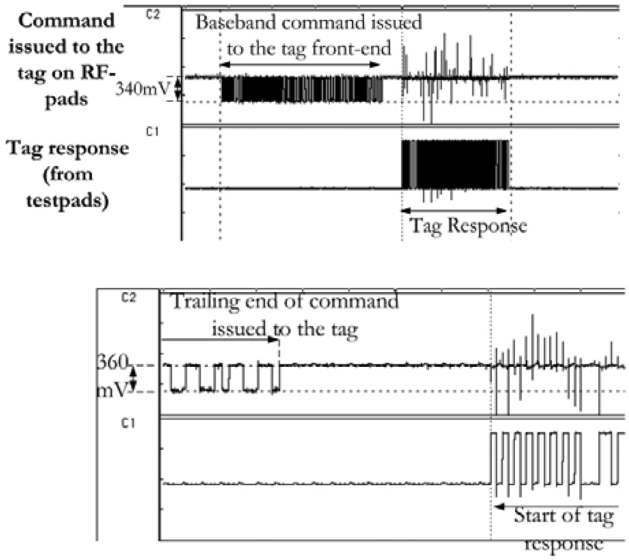

Fig. 19. Oscilloscope plots of baseband commands issued to the chip. Top shows a regular ISO-180006B command issued to the tag(after it is in the "full-power" mode) and the response of the chip(which is brought out on a testpad) is shown. Lower figure is a close up of the top figure showing portions of the command issued as well as the response from the chip.

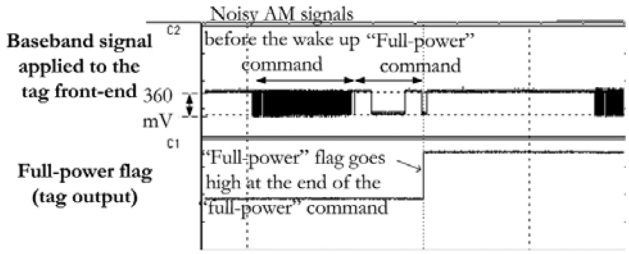

Fig. 20. Oscilloscope measurements of a series of bit patterns issued to the chip. Note that the chip does not falsely decode any of the bit streams as a "full-power command" and correctly decodes the "full-power" command.

the base-station). Fig. 20 shows the "full-power" command issued to the tag. Prior to the "full-power" command a bit stream is sent to see if it can trigger a false wakeup on the chip. The full-power flag (which is brought out on a testpad and is shown in Fig. 20) goes high only after the tag has received a valid "full-power" command and stays high as long as the tag is in the "full-power" mode. Fig. 21 shows the spectrum of the backscattered signal from the tag, while the reader is transmitting a CW carrier; the plot was measured using HP-89441A Vector Signal Analyzer using an RBW of 1 kHz. Fig. 22 shows S11 for the chip front-end in the frequency range 2.2 to 2.65 GHz, when the incident source power is 0 dBm using a HP8719C Vector Network Analyzer. The bare die was wirebonded to landing traces and encapsulated with a glob; the impedance of the package was measured across the landing traces. Fig. 23 shows the front-end *I–V* curve. The regions where the two stages of voltage regulation are operational are shown in the figure.

B. Tag Random Number Generation and the Binary Sort Algorithm

It is critical to evaluate the random number generation on the tag. A faulty random number generation algorithm will greatly reduce the identification rates of tags in the field; additionally for

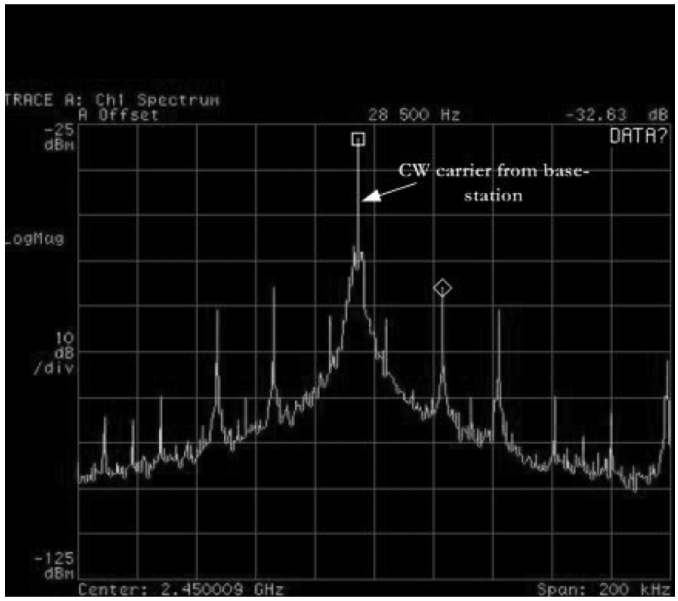

Fig. 21. Frequency spectrum of the tag response measured with an HP-89441A, using a RBW = 1 kHz. The tag is located 11 in away from the base-station with an inline attenuation in the forward path of 11 dB.

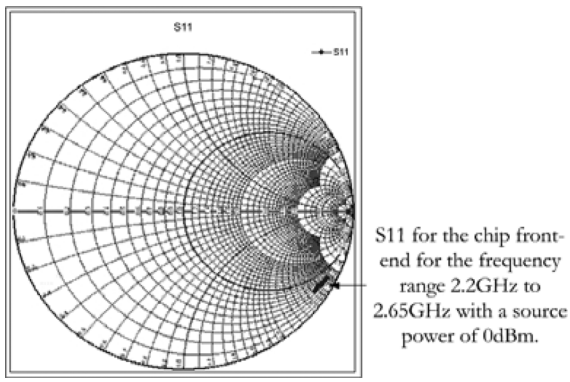

Fig. 22. S11 plot for the chip front-end, measured with an HP8719C vector network analyzer.

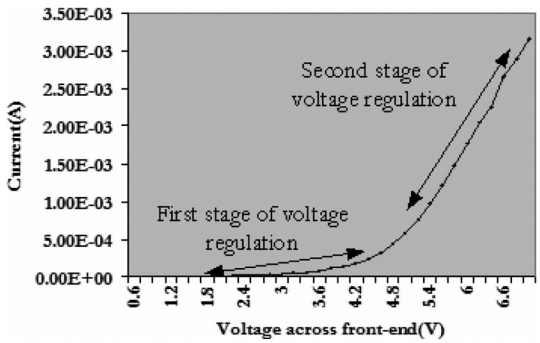

Fig. 23. Experimentally measured *I–V* characteristics of the front-end. The *I–V* curve shows the regions where the two stages of voltage operate.

a given number of tags, there will be nonuniformity in the identification of tags. The experimental setup consists of five tags in the field, which are all well energized. The tags are queried by a basestation in such a manner that if the difference in the counter values of any tag is greater than 2, then those tags will not be identified (e.g., if Tag 1 has a counter value of 2 and Tag

TABLE I
NUMBER OF TIMES A TAG WAS IDENTIFIED OVER 30-S INTERVAL

Tag Number	*No. of times identified*
Tag 1	287
Tag 2	286
Tag 3	287
Tag 4	288
Tag 5	289

TABLE II
SIMULATED CURRENT CONSUMPTION FOR VARIOUS BLOCKS

Module	*Standby Current(nA)*+
Voltage Reference	130
Receive/Transmitter	0
BaseBand Amplifier	125
ICO Oscillator	90
Random Roll Oscillator	0
Battery Wakeup Oscillator	83
Active Power	12uA* x 0.1% = 12
TOTAL	440

The average current consumption for a read type operation is 12uA[5]
+All the blocks are current driven and hence standby current is relatively independent of voltage

TABLE III
SUMMARY OF EXPERIMENTALLY MEASURED CHIP CHARACTERISTICS

Parameter	*Value*
Tag impedance at 2.4GHz	50-j276
Tag impedance at 915MHz	92-837j
Range at 2.4GHz	3.5m
Current consumption (nA)	700(@1.5V), 800(@2V),880(@2.5V)
RF threshold power	-19dBm

2-4 have a counter value greater than 4, then tags 2–4 will not be identified in a given round). Each round will identify a tag not more than once. Table I gives the number of times the 5 tags were identified in a 30 second interval. It can clearly be seen that the numbers are very close for each tag, thereby confirming that the random number generation algorithm is working very well.

C. Tag DC Power Consumption

Table II shows the simulated power consumption for the circuit blocks in our chip. The total simulated power consumption is 440 nA; however the measured value was close to 700 nA at 1.5 V. Table III shows the experimentally measured current drawn by the tag at different voltages. Switching power consumption (due to rail to rail voltage swing) at a supply voltage V is proportional to V^2 and the resultant extra switching current I_{switch} is proportional to V (since $VI_{\text{switch}} \propto V^2$). This gives an extra switching current of approximately 200 nA/V and at 1.5 V, the switching current drawn is 300 nA. The nonswitching current consumption is approximately 400 nA and is very close to the simulated values. Note the on-chip circuitry itself is current limited and hence makes no contribution to the switching power. The extra switching power consumption comes from the test-pad drivers that bring out internal signals on test-pads (for debugging and testing). For calculating power drawn by the tag in "full-power" mode (Table II), a 0.1% usage (i.e., 0.1% of the time, the tag is in the "full-power" mode and 99.9% of the time the tag is not being interrogated by a reader) model was assumed- this represents 788 million read type operations [3] which is considerably more than the total number of read operations usually done on one tag over its lifetime (10 years).

D. Tag RF Threshold Power

The tag impedance measurement was done with an HP 8719 Network Analyzer; "Cascade" Fixed Pitch probes were used to make contact with bare die. Impedance was measured at various frequencies and power levels under unmatched conditions. The chip was powered with an RF source (Network Analyzer) and the rectified dc voltage was measured. The chip threshold power is reached when the on-chip rectified voltage is 0.2 V (this is sensitivity spec for the on-chip amplifier). The RF threshold power measured was -19 dBm at 2.45 GHz. At this power level, the measured impedance was 50-j276. The rectified voltage developed on the chip at this power level and impedance according to (6) is 0.2 V, confirming the experimental measurement. The tag impedance measured at 915 MHz is 92–837 j with a source power of 5 dBm.

E. Tag Range

Tag range measurements were done in a Tescom 5060 B Broadband TEM cell and the tags showed a range of 3.5 m with a power of 4 W EIRP at 2.4 GHz(as required by FCC for unlicensed operation in the 2.4 GHz band). When the tag operates in the passive mode (without a battery), a range of 0.7 m is obtained. The tag shows a free space range in excess of 3.5 m at 2.4 GHz. The theoretical range as predicted by (6) is 3.51 m(with $Vth = 160$ mV, which was the measured threshold voltage for the particular tag). We note that the experimental range is very close to the theoretical range based on the tag front-end impedance. At 915 MHz, based on the experimentally measured tag impedance (92-j837 in Table III) and the threshold spec of the tag (200 mV), the theoretical minimum range is 24 m.

VI. SUMMARY

A fully integrated battery powered RFID chip was demonstrated for the first time. The battery chip can function in a novel dual mode of operation—both passive and battery powered. This removes one of the major drawbacks of currently available active tags—the fact that active tags cannot be re-used once the battery dies out and any valuable data on the tag is lost forever. The IC is built on a 1 μm digital CMOS process with dual poly layer with read/write EEPROM and Schottky diodes. The tag draws a current of 700 nA at 1.5 V (this design actually only draws 400 nA if circuitry used for purposes of lab evaluation are removed from the device; currently internal signals are multiplexed to test pads for observation of the ISO 18000-4 B protocol and are not used in the field) in the "low-power" mode. The low current consumption allows for a tag lifetime in excess of 10 years with a tiny 100-mA·h battery. As a result the tag has a form-factor close to that of a passive tag. We provide a theoretical derivation for the range of a tag given its impedance and draw qualitative conclusions on maximizing the tag range; the tags have shown ranges in excess of 3.5 m at 2.45 GHz with an attached battery and a range of 0.7 m in the passive mode of operation. Tags have an RF threshold power

of −19 dBm at 2.45 GHz, which is the lowest ever reported threshold for RFID tags that operate in the Microwave band. The low threshold was achieved by the use of a battery to power circuitry and minimizing the power absorbed from the front-end. To minimize the power drawn by the tag over its lifetime, the tag was architected to operate in a "lower-power" mode. We calculate power consumption of this device using a conservative estimate of 0.1% usage over the lifetime of the tag. This design maximizes the useful life of the battery powered tag by reducing current consumption during the 99.9% time the tag is not being interrogated by a reader. A tiny 100-mA·h battery can power this tag for over 10 years without loss of functionality of this tag including read/write capability to the onboard 1-kb EEPROM. Detailed descriptions of the chip architecture and circuit schematics were provided. The chip uses a broadband Schottky diode based front-end and thus it can be used both in the Microwave (2.45 GHz) and the UHF band (915 MHz). In the UHF band, the tag shows a theoretical range of 24 m. We have provided detailed schematics and explanation for the operation of various circuits in the "full-power" mode. The binary sort algorithm, random number generation and the clock recovery architecture were explained in detail. Except for the battery and antenna board, the tag does not use any external components. Overall, this is a very promising design that can be used for various RFID applications.

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