A Building Block for Nuclear Medicine Imaging Systems Data Acquisition

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I. INTRODUCTION

Developing new detector designs for PET and SPECT imaging systems often leads to problems in adapting existing data acquisition electronics to the requirements for the new devices. As we developed our dMiCE and cMiCE detector concepts [1,2], we found that our existing electronics was inadequate to the task and launched a design effort we have termed our Phase II electronics [3]. Here we report on the implementation and evolution of the Phase II system.

II. PHASE II SYSTEM DESIGN AND TESTING

A. System design

The basic approach was to minimize analog processing and move as much pulse processing as feasible into an FPGA. To allow easy adaptation to different detector, we designed the system around a digital processing board (the Phase II board) which is then connected to the detectors with a separate analog adapter board. The analog board provides power and any local control needed to the detector and sends differential signals to the Phase II board.

Figure 1 is a block diagram of the Phase II board. It is designed to accept either 64 channels of differential analog signals (which are then digitized with 65 MHz ADCs) or 64 channels of serial signals from a detector adaptor board. The board also has one high speed (> 300 MHz) ADC channel for those detectors that provide a fast timing pickoff signal. The Phase II board is designed around a family of high performance FPGAs from Altera, and we have developed a wide range of pulse integration, timing, and processing algorithms for the device [4-7].

Other features of the board include several SPI bus and temperature monitoring connectors, as well as expansion connectors for daughter boards for future requirements. Switches allow setting ID numbers for the boards. Due to the requirements for the statistical estimator for the cMiCE

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Figure 1: Block diagram of the main components of the Phase II acquisiton node board.

detector [6], the board also includes 380 Mbytes of static random access memory. As described in [3, 8] the cards can be setup to serve several functions in a scanner system including serving as a master coincidence controller, an acquisition node taking data directly from detectors, or as a acquisition node that is taking data from other Phase II cards that are in turn connected to detectors (a modified star topology). The initial design used FireWire for the host to board data transfer and commands. We are currently implementing USB 2.0/3.0 support via a daughter board and will incorporate that circuitry on the main board in the next revision (expected by August 2012). The FPGA also is configured with the NIOS II software based embedded processor for general control, processing of commands from the host, and communications between the cards. А megabyte of FLASH ROM is included for NIOS software and other data needed to be loaded into the static RAM supporting the FPGA. The FPGA is loaded at power up from an Altera load device and additional FLASH ROM. JTAG connectors are provided for programming and testing. More details are included in [3,8]. Figure 2 depicts the top side of the Phase II board.

B. Initial testing

Figure 3 shows the board setup for testing with a cMiCE detector. The overall performance met expectations and the time to debug the card was less than we had anticipated. Once all of the components were confirmed to be operating properly, simple Verilog code was written and combined

This work was supported in part by the NIH grants NIBIB EB001563, NCI CA136569, and DOE grant DE-FG02-05ER15709.



Figure 2: Top of the Phase II electronics board showing the FPGA, half of the memories and ADCs (the other memories and ADCs are on the bottom side of the card).

with C code in the NIOS II soft embedded processor to begin testing the card with real data. For these first tests, a prototype detector adapter board was fabricated to provide amplification and conversion of signals to differential pairs from a cMiCE detector utilizing a 64 channel Hamamatsu H8500 PMT. This setup allowed testing of the revision 1.0 Phase II board by recording event by event data digitized from all 64 analog inputs. Figure 4 depicts one of the first tests done with signals form a cMiCE PMT based detector. A single event is show with the digitized outputs from each of the 64 anodes (the grid of small plots) and a zoomed plot of the anode with the largest signal.



Figure 3: Phase II board connected to a cMiCE detector with new adapter cMiCE adapter boards.

III. DISCUSSION AND CONCLUSION

The board is meeting its design specifications and is now being used to develop a pre-clinical scanner and also a human breast scanner based on the cMiCE detector concept. Additional projects include licensing the card to a company for use in their gamma ray imaging systems as well as implementing an easily configurable I/O system to support a variety of bus types – with the first major revision being the support of USB 2.0/3.0 will be completed later this year. Along with the card, we have a reconfigurable software tool for list mode acquisition that will support the bus types the Phase II card is configured for. Standard command and control code has also been written for the embedded processor on the Phase II board to allow easy adaptation to



Figure 4: Example of a single event from a cMiCE detector with a 64 channel PMT using the prototype cMiCE adapter board (not the new boards shown in Figure 3)showing all 64 spectra and an enlargement of the anode with the largest signal.

many different acquisition topologies -a few examples of which is shown in Figure 5.

REFERENCES

- Champley, K.M., Lewellen, T.K., MacDonald, L.R., Miyaoka, R.S., Kinahan, P.E.: "Statistical LOR Estimation for High-Resolution dMiCE PET Detector", Phys. Med. Bio. 54, pp. 6369-6382 (2009).
- [2] Li, X., Hunter, W.C.J., Lewellen, T.K., Miyaoka, R.S.: "Spatial Resolution Performance Evaluation for a Monolithic Cyrstal PET Detector with Cramer-Rao Lower Bound", IEEE Nuclear Science Symposium and Medical Imaging Conference (2010).
- [3] Lewellen, T.K., Miyaoka, R.S., MacDonald, L.R., Haselman, M., DeWitt, D., Hauck, S.: "Evolution of the Design of a Second Generation Firewrie Based Data Acquisition System", IEEE Nuclear Science Symposium and Medical Imaging Conference (2010).
- [4] Hasleman, M.D., Hauck, S., Lewellen, T.K., Miyaoka, R.S.: "FPGA-Based Pulse Pileup Correction", IEEE Nuclear Science Symposium and Medical Imaging Conference (2010).
- [5] Haselman, M., Hauck, S., Lewellen, T.K., Miyaoka, R.S.: "FPGA-Based Pulse Parameter Discovery for Positron Emission Tomography", IEEE Nuccear Science Symposium and Medical Imaging Conference pp. 2956-2961 (2009).
- [6] Johnson-Williams, N.G., Miyaoka, R.S., Xiaoli, L., Lewellen, T.K., Hauck, S.: "Design of a real time FPGA-based three dimensional



Figure 5: Examples of some of the bus topologies that can be supported with the Phase II card.

positioning algorithm", Nuclear Science Symposium Conference Record (NSS/MIC), 2009 IEEE pp. 3652-3659 (2009).

- [7] Haselman, M.D., Hauck, S., Lewellen, T.K., Miyaoka, R.S.: "Simulation of algorithms for pulse timing in FPGAs", Nuclear Science Symposium Conference Record (NSS/MIC), pp. 3161-3165 (2007).
- [8] Lewellen, T.K., Miyoka, R.S., MacDonald, L.R., DeWitt, D., Hauck,

S. "Evolution of the design of a second generation FireWire based data acquisition system". Nuclear Science Symposium Conference Record (NSS/MIC), pp. 3994-3998 (2011).