

Evolution of the Design of a Second Generation FireWire Based Data Acquisition System

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Abstract: Developing new detector designs for PET and SPECT imaging systems often leads to problems in adapting existing data acquisition electronics to the requirements for the new devices. As we developed depth-of-interaction detector designs based on both discrete crystal arrays (dMiCE) and monolithic crystals (cMiCE) concepts, we found that our previous electronics design was inadequate to the task and launched a design effort we have termed our Phase II electronics. The system is based on a basic card design (the Phase II board) that has a large field programmable gate array (FPGA) with sufficient static RAM to support a variety of pulse processing algorithms our group has developed – including timing estimation, pulse integration with pileup correction, and statistical estimation of the event location in the detector. The Phase II board can be configured to take on several roles, including a master/coincidence controller, an acquisition node handling up to 64 channels of analog data digitized at 65 MHz and one channel digitized at >300 MHz, an acquisition node supporting up to 64 serial data inputs (e.g., from devices like digital silicon photomultipliers), or as an acquisition node that takes in data from other Phase II boards in a star configuration to expand the number of detector modules the system can support. The current implementation is based on FireWire (limiting the total number of acquisition nodes directly connect to the bus to 62), but future versions are planned to support USB and PCIexpress. Here we report on the testing of the first prototype Phase II main board supporting a 64 channel cMiCE detector and describe the current development plans for the system.

I. INTRODUCTION

We have previously reported on the design of a new data acquisition system (Phase II) which has evolved from the experience gained with our first FireWire based system [1]. The new system is needed to address challenges presented by the several different detector designs being developed in our laboratory [2-4]. It implements many of the FPGA pulse processing algorithms we have previously described [5-8] and provides a large number of options for different applications.

Figures 1-4 depict examples of the four major detector designs currently being utilized in our laboratory. The original cMiCE module is based on a multi-anode photomultiplier tube (PMT) coupled to a monolithic crystal. It requires 64 channels of readout along with a timing pickoff channel. In

addition, the module is designed to be used with statistical based position algorithms to estimate the x, y, and z coordinates of the event. Our designs call for those algorithms to be implemented at the detector module level to further reduce the amount of data required to be sent to the host computer. Those algorithms have been developed and implemented in FPGAs [8]

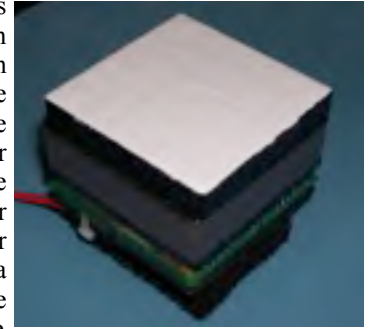


Figure 1: cMiCE detector module, requires 64 readout channels plus a timing pickoff channel.

The dMiCE approach (using controlled light sharing

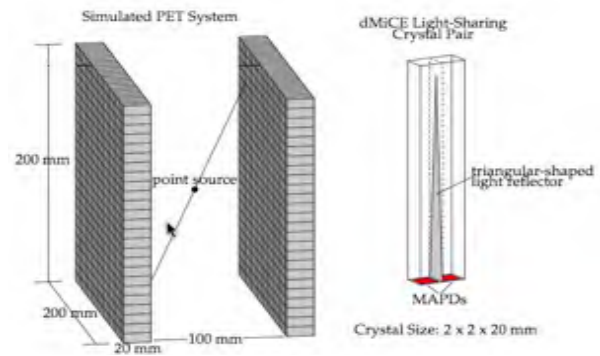


Figure 2: dMiCE detector module requiring more than 40 channels of readout.

between crystal pairs) requires individual readouts for each crystal pair (Figure 2). The current module designs are based on arrays of 10x10 to 20x20 and will use SiPM devices for the light collection. To reduce the number of readout channels, a row/column/diagonal summing ASIC [9] is under development that would reduce the number of channels to be digitized for a 20x20 array to 60 plus a time pick off channel. The timing channel will be from a current pickoff on the common bias voltage to the SiPM array.

A variant on the cMiCE approach is shown in Figure 3. For this design (termed SES) the sensor array is put on the entrance surface of the monolithic crystal, closer to where the majority of first interactions occur. The result is in an improvement in the estimation of the position of the event. The initial versions of this design use an 8x8 array of SiPMs mounted on a flex circuit to allow routing of the signals to the back side of the detector module where the connectors and impedance matching networks are located. As with the original cMiCE module, 64 read out channels and one timing channel will be utilized. The timing channel is provided by a current pickoff of the common bias supply to the SiPM array.

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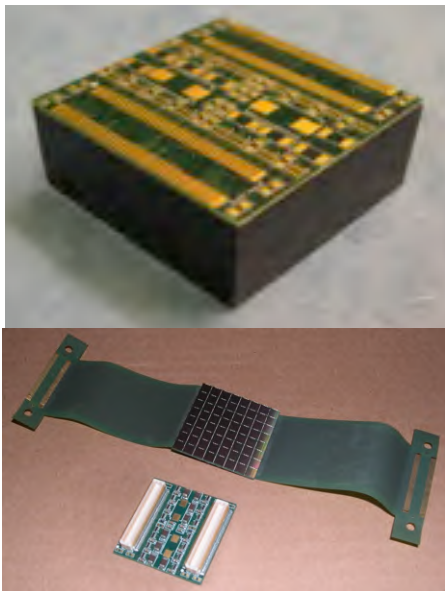


Figure 3: SES cMiCE detector module (sensors on front surface of the monolithic crystal) with flex circuit for routing signals to the back side of the module.

However, future versions may go to a larger SiPM array to obtain better sampling of the light spread functions, in which case we plan to use the row/column ASIC [9] to reduce the number of signals to be processed.

Another detector design is shown in Figure 4 where we are using segmented crystals (tapered) in the transaxial direction and continuous decoding in the axial direction. The current module design requires 16 channels of readout, again with a timing pickoff provided by a current pickoff on the SiPM array common bias supply.

Our original FireWire based acquisition system does not have the capacity to effectively support all of these various module designs. We have investigated other projects such as the OpenPet initiative [10], but the FPGA capacity for such options were not adequate to support the estimation algorithm requirements for the cMiCE and SES detector designs. Thus, we undertook the design of a new system based around a very flexible digital processing card that relies on performing all of the pulse processing (timing, integration, baseline correction, pileup correction, and position estimation) in a large FPGA.

II. MATERIAL AND METHODS

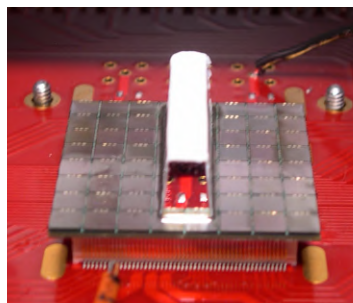
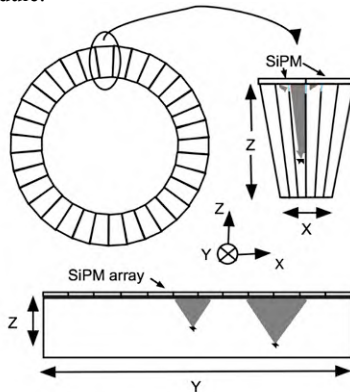


Figure 4: TSC detector module prototype (2x8) requiring 16 channels of data per detector.

We have separated the electronics design into two major subsystems: analog and digital. The analog subsystem boards are specific for each detector type supported. Typically an analog board has differential drivers for the signals to the digital board, detector power supplies, and a circuit to provide a common timing pickoff signal for whatever photosensor array is being used. The analog boards also have SPI buses for controlling the detector bias supply and any other logic on the board (such as an ASIC).

Briefly, the digital board contains the analog to digital converters (ADC) for the detector signals, the bus support to the host computer (FireWire for the current version), small peripheral interface buses (SPI) for devices on the analog subsystem as well as communications to other digital boards, and the FPGA with additional external memories. The basic function of the board is to digitize the detector signals, perform the required pulse processing, and then send the data to the host computer. Since design and layout of such a board is a major undertaking, we decided to make it very flexible and to allow support of many different acquisition topologies, expansion port for future additions or alternative bus support to the host (e.g., USB), and to support new digital SiPM devices such as those being developed by Philips [10].

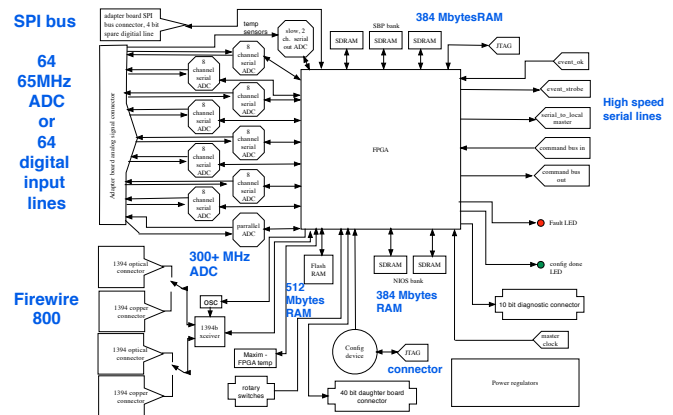


Figure 5: Block diagram of the Phase II card.

A block diagram of the current version of the digital board is shown in Figure 5. The current printed circuit board (PCB) is 216 mm long and 104 mm wide and consists of 12 layers. The schematic layout (in particular the pin assignments for the FPGA) had to be done iteratively with the PCB layout to reduce the number of layers. Such a process allows for minimization of path lengths and reduces the number of required layers in part by reducing the number of traces that need to cross over each other. Part of the process is a measurement of the trace lengths and calculation of both time skew and bandwidth capacity (which is also driven by the trace geometry) to assure that the performance targets for the board can be maintained. For example, each serial ADC integrated circuit contains eight discrete ADCs, each digitizing at rates up to 70 MHz from a common clock. Each IC then connects to the FPGA with eight serial data lines synchronized to a common clock. The data rate on each serial line when digitizing at 70 MHz is 840 mbps. Figure 4 is a top view of the current board along with an “x-ray” view of the PCB layout (all layers) from the Eagle software tools used for the design. The other side of the board (not shown) is similar in appearance to the top view but without the FPGA mounted (it

includes serial ADCs, memories, and the configuration IC). This board uses an Altera Stratix III FPGA in a F1517 package. Selection of the F1517 package allows a variety of specific Altera FPGAs to be used so that any one board can be configured with the FPGA best suited for the application in terms of capacity and cost. For the current board, we are using a Stratix EP3SL200 which is a high end member of the Stratix III line of FPGAs and has the needed number of phase lock loop (PLL) elements required to support the ADC and memory I/O requirements.

The left side top (Figure 7) of the card includes five SPI bus connectors (for use by the analog cards, and/or communications to other digital cards), temperature analog inputs to a dual channel serial ADC, an alternative (one cable) connector for the 5 SPI buses, a connector to the parallel AC (intended for time pick off signals), and a connector for two channels of logic triggers intended for alternative timing triggers from the analog card. The detector signals are routed to connectors on either side of the serial ADCs. The outgoing FireWire signals, the master clock in, the event present and event accept control lines [1], a SPI bus for command/control from the maser controller, and the power are all on the right side of the card.

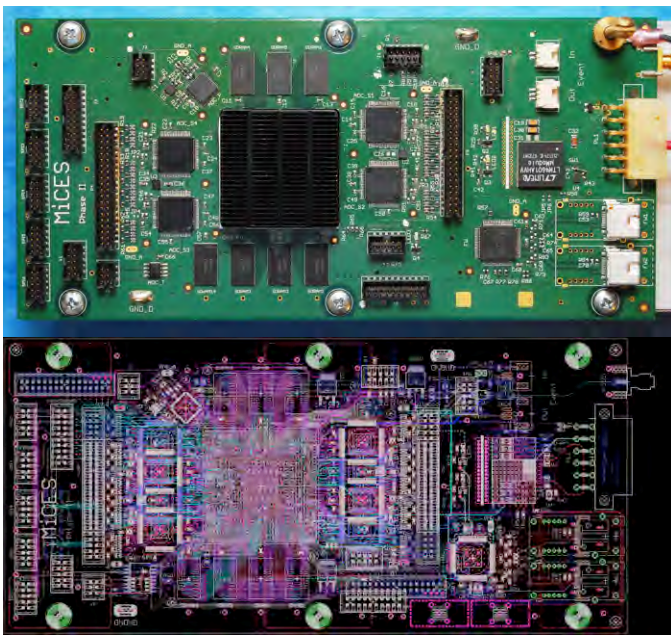


Figure 5: Phase II card top view and and the X-ray image (generated by the Eagle layout software) showing the 12 layers of traces.

When cooled air is required for operation (such as in our MRI insert scanner designs), the air is introduced along the bottom edge of the card and removed along the top edge of the card assuring good flow across the FPGA heat sink and the memories. The current TI FireWire transceiver chip is located at the bottom right of Figure 5. Next to the FireWire transceiver chip are pads for either copper wire FireWire connectors (which are installed in Figure 5) or ethernet optical transceiver/connectors for FireWire over optical or other protocols. There is also a local oscillator that is used to run the card when a master clock is not being supplied to the card (R&D or stand alone operation). The FPGA generates the higher speed clocks needed for the various subsystems.

For future expansion and testing there are two daughter board connectors (16 bits each) on the bottom of the board, a general purpose test/auxiliary signal connector (10 bits) on the front side of the board, a JTAG connector for the FPGA, a JTAG/active serial connector for the load device, two rotary switches connected to the FPGA (e.g., setting board identification data), and several LEDs that monitor configuration status.

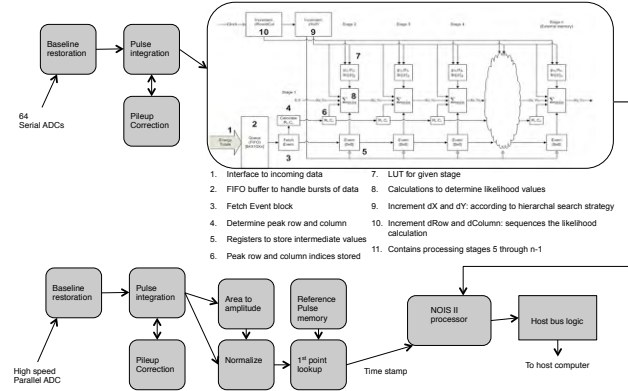


Figure 6: Diagram of the FPGA logic used for the cMiCE detector module.

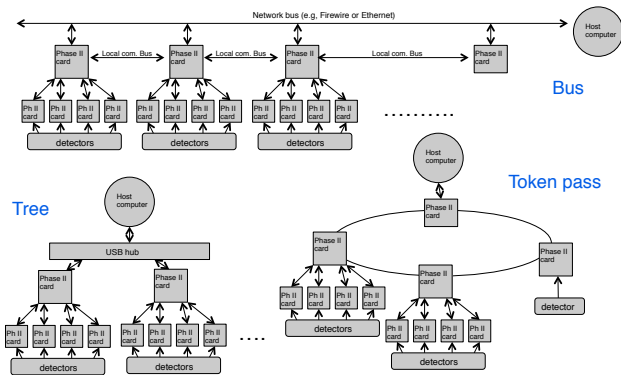


Figure 7: Examples of some of the bus topologies that can be supported with the Phase II card.

The cMiCE support requires external memory support for the FPGA and the board is equipped with 380 Mbytes of static random access memory (RAM) for that purpose. An additional 64 Mbytes of static RAM is included for use by the NIOS II embedded processor programmed into the FPGA. For loading the FPGA code and the look up tables used by the cMiCE event estimation algorithms, 512 Mbytes of FLASH RAM is also installed on the board, along with an Altera load device (EPCS128). The serial ADCs are currently eight Texas Instruments ADS5272 running at 60 MHz (sending data to the FPGA at 720 mbps per output), providing the 64 channels of event input. The high speed parallel ADC for the timing signal is an Analog Devices AD9211 currently running at 300 MHz. An example of how the FPGA is configured for the cMiCE detector is shown in Figure 6. Even this application only uses about 30% of the FPGA logic.

Figure 7 depicts some of the many topologies the digital card can be used to support. The use of the large FPGA and NIOS embedded processor provides a system designer with a wide range of options to adapt the card to a particular application.

III. EXPERIMENTAL RESULTS

The first revision of the board has undergone initial performance testing. Figure 8 shows a typical testing configuration using two cMiCE detectors. Figure 9 shows the single event data from a cMiCE detector utilizing all 64 slow ADCs for the channel data and the fast ADC for the timing data. Figure 10 shows a comparison of summing all 64 channels of “slow” data versus the fast timing pickoff data (a common anode signal from the PMT) as recorded by the Phase II digital board. The data not only confirm the correct operation of the ADCs, but also confirms that the time skew and general ADC decoding logic in the FPGA is operating

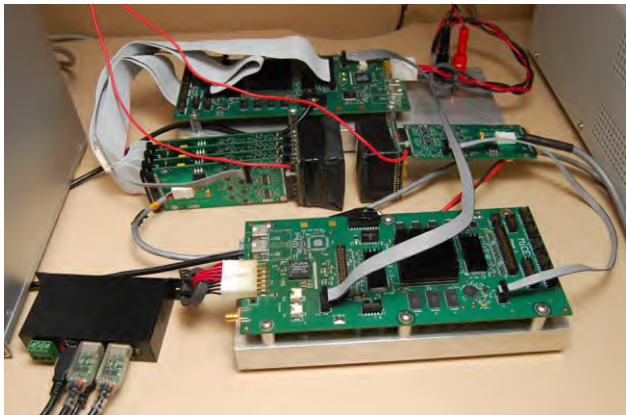


Figure 8. Test bench with two Phase II digital boards and two cMiCE detectors (left detector with full 64 channel readout, right detector setup for timing only).

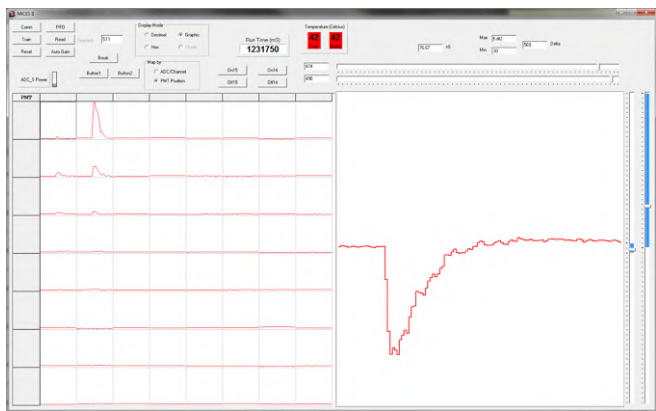


Figure 9: Example of a single event in the cMiCE detector (grid of 64 channels on the left) and the timing pulse (plot on the right) as recorded by the Phase II digital card.

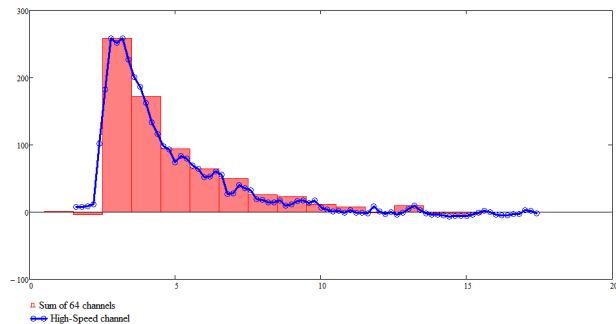


Figure 10: Comparison of the summed slow ADC channels and the high speed timing ADC for a single event from the cMiCE detector as recorded by the Phase II digital card.

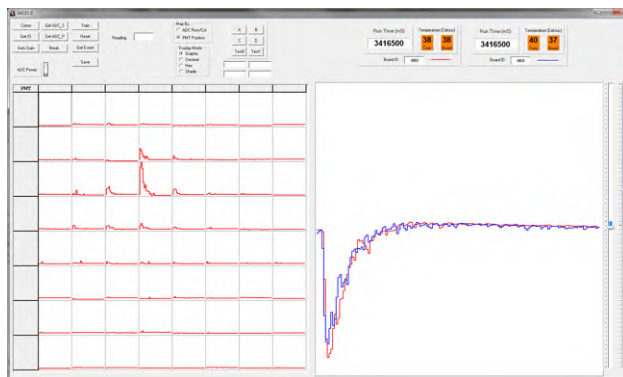


Figure 11: Data from a single event for the test configuration of Figure 8. The 64 channels of the left PMT are shown on the left and both timing pickoff channels are shown on the right. In this case, the FPGA logic utilized the SPI busses to notify the paired boards that a coincidence event occurred.

correctly. Figure 11 depicts a coincidence event as recorded by the digital card in the test configuration of Figure 8. The timing measurements are still being conducted with the fast ADC. We have included a figure from a prior report [5] in Figure 12 since we have confirmed that the current digital cards conform to the timing data previously reported as a function of the bandwidth limitation of the analog signals. We are now working on a new timing pickoff board that provides a higher bandwidth signal to the fast ADC to explore the timing capabilities of the current configuration.

III. DISCUSSION

The first revision of the board has been fabricated and is performing as designed. The card can be adapted for a wide variety of applications by selection of which components to mount on the board and the selection of the specific FPGA to

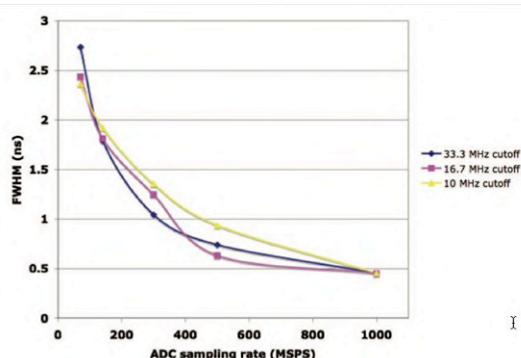


Figure 12: Timing resolution as a function of the analog pulse bandwidth and ADC sampling rate for the timing algorithms implemented in the FPGA. Taken from reference [5] and being verified on the current digital card.

be used. The Altera F1517 package used in our design is used for several devices in the Stratix III and IV series of devices - allowing several pin-compatible options for the specific FPGA used for a given application.

Flexibility is a major design goal for the many I/O options on the board. For example, the SPI connectors can also be used as general purpose signal lines - they are not restricted to

being defined as SPI buses. In the same way, we can replace the serial ADCs with small ball-grid boards that simply connect the differential inputs directly to the FPGA and can be used, for example, as 64 serial input channels for devices such as the Philips digital SiPM.

While our current version is based on the FireWire 1394b protocol for communication to the host, the card includes an expansion connector that can be used for other bus standard such as USB. In fact, one user is already designing such a daughter card. The pinouts on the existing card for the FireWire connectors also supports a range of Ethernet connectors - both copper and optical. Thus, bus topologies based on Ethernet can easily be implemented. The flexibility is obtained in large part by having the protocol layers in the FPGA rather than in the transceiver chips. That, coupled with the flexibility of how the NIOS II soft embedded processor, allows the board to support just about any protocol for connection to the host computer.

A new version of the board is already being fabricated with some small improvements in terms of protection from incoming power fluctuations and adjustments for changes in available IC components. Future directions include investigating a general purpose I/O daughter card to allow easy conversion from FireWire to USB or other standards such as Intel's Thunderbolt Bus system.

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