Evolution of the Design of a Second Generation FireWire Based Data Acquisition System

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Abstract: **Our laboratory has previously reported on the basic design concepts of an updated FireWire based data acquisition system for depth-of-interaction detector systems designed at the University of Washington. The new version of our data acquisition system leverages the capabilities of modern field programmable gate arrays (FPGA) and puts almost all functions into the FPGA, including the FireWire elements, the embedded processor, and pulse timing and integration. The design is centered around an acquisition node board (ANB) that includes 64 serial ADC channels, one high speed parallel ADC, FireWire 1394b support, the FPGA, a serial command bus and signal lines to support a rough coincidence window implementation to reject singles events from being sent on the FireWire bus. Adapter boards convert detector signals into differential paired signals to connect to the ANB. In this paper we discuss many of the design details, including steps taken to minimize the number of layers in the printed circuit board and to avoid skewing of parallel signals and unwanted bandwidth limitations.**

I. INTRODUCTION

We are designing a second generation data acquisition system to support several positron emission tomograph (PET) designs being developed at the University of Washington. It is based on our experience with the original MiCES electronics concepts [1]. However, the new system is more compact and designed to support both our continuous detector development efforts (cMiCES) and our discrete crystal depth-of-interaction detector designs (dMiCES) [2-4]. It implements many of the FPGA pulse processing algorithms we have previously reported on [6-8].

The dMiCE design uses light sharing between crystal pairs and a single ended readout to decode depth-of-interaction. For pre-clinical applications, the new dMiCE detectors are being designed with < 1mm pitch requiring a fine pitch SiPM array with a very large number of readout channels. The current prototype detectors are on a coarser pitch using currently available 8x8 silicon photomultiplier (SiPM) arrays. To support the final designs, we are developing an application specific integrated circuit (ASIC) that will support up to a 20x20 SiPM array with a row-column-diagonal summing scheme to reduce the number of channels from 400 to < 64.

The cMiCE design is based on monolithic crystals with single sided readout either on the front or back side of the crystal block (Figure 2). The current prototypes use 8x8 photosensor arrays (photomultiplier and SiPM versions have been built). For finer sampling, smaller SiPM arrays are being considered and would use the new ASIC to reduce the number of channels. The net result of these detector and ASIC designs is that our new electronics needs to support up to 64 channels of array signals with a common timing channel. We have also considered devices such as the new Philips digital SiPM arrays which use serial outputs and have included support for such devices in our general design specifications.
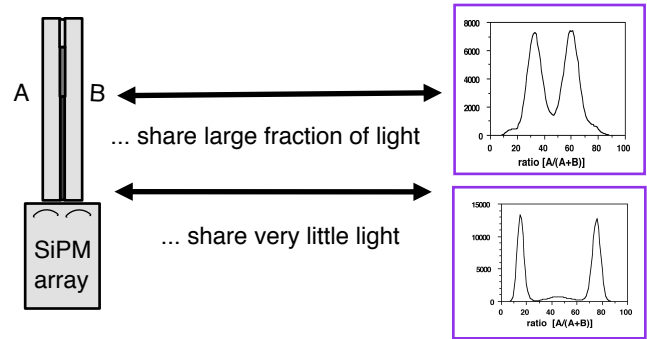

Figure 1: Basic dMiCE detector concept using light sharing and single ended readout to provide DOI information
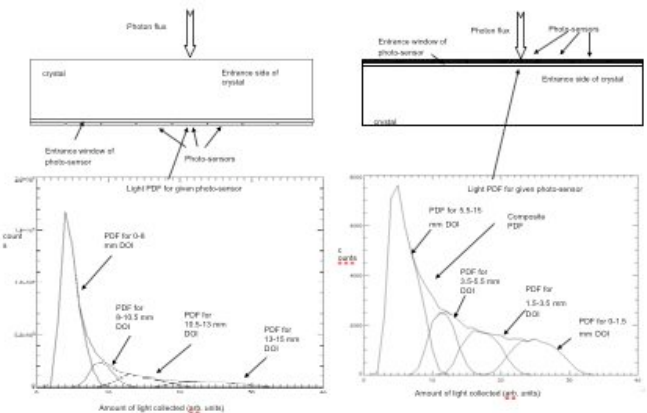

Figure 2: cMiCE design concepts. Using a statistical estimation algorithm, the x,y,z position of an event is estimated from the light distribution. All of the designs are based on single sided readout with the sensors either on the back or front of the crystal block. The front side configuration results in better DOI (z coordinate) estimation.

Our first FireWire acquisition system for the MiCES scanner does not have enough capacity in the FPGAs and the boards are too bulky. Before undertaking a new electronics

development effort we survived commercial offerings and the Open PET consortium effort [9] for alternatives. However, the demands for the cMiCE statistical estimation algorithms [8] requires a larger FPGA and more support memory than is available on the commercial devices we found nor the Open PET designs . Further, we wanted a relatively compact board that was designed for operation within the bore of a MRI imaging system. After the survey of options, we proceeded with our new electronics system based on what we learned in our original FireWire based system and the requirements for the support of the new ASIC we are designing and the cMiCE detector designs.

II. MATERIAL AND METHODS

As we reported previously, the basic system design is built around a multi-purpose board design – the acquisition node board (ANB) - and we use the term Phase II electronics to describe the entire development effort [10]. We have separated the electronics design into two major subsystems analog and digital. The ANB board is the digital subsystem for all of various detector designs (present and future). The analog subsystem boards are specific for each detector type supported. Typically an analog board has differential drivers for the signals to the ANB, detector power supplies, and a circuit to provide a common timing pickoff signal for what ever photosensor array is being used. The analog boards also have SPI buses for controlling the detector bias supply and any other logic on the board (such as an ASIC).

Briefly, the ANB board contains the analog to digital converters (ADC) for the detector signals, the FireWire transceiver integrated circuit (IC), small peripheral interface buses (SPI) for devices on the analog subsystem as well as communications to other ANB boards, and the FPGA with additional external memories. The basic function of the board is to digitize the detector signals, determine pulse timing and perform pulse integration, and then send the data to the host computer via the 1394b FireWire bus.

When used in a scanner system, one of the ANB boards is also configured as a master controller and a coarse coincidence processor. The coarse coincidence timing is used to reject events that we know will not be processed by the host computer where the final coincidence timing is determined. Similarly, the system uses options in the logic in the FPGAs to geometrically qualify events depending on the detector configuration being used and the post processing to be utilized. The ANB can also be used as a local controller mode to support a star topology under each FireWire node to allow for a much larger number of detectors in the system than there are FireWire nodes [9]. In this configuration, an ANB is configured as a "local master" and connects up to four additional ANBs that can either be acquisition nodes (with ADCs) or a second layer of local masters. The communications between the local master connected to the FireWire bus is via high speed serial connections. The FPGAs on the local masters package the data from the acquisition nodes for transmission to the host computer. The coarse timing window information is passed from the coincidence controller to the acquisition nodes via the local masters.
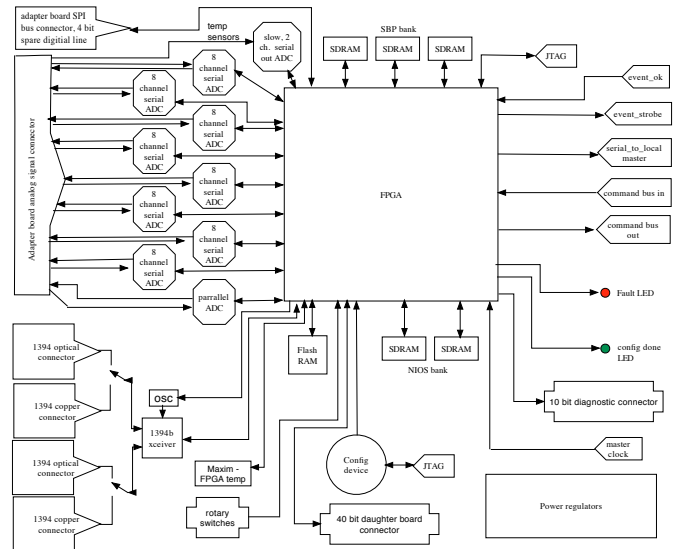

Figure 3: Block diagram of the main components of the Phase II acquisiton node board.

Figure 3 shows a block diagram of the ANB. When used as a master or local controller the ADCs are replaced with jumper blocks to allow use of the signal connectors for high speed serial communications to the other boards in the system [9]. The components have been selected both for the needed functions to handle dMiCE and cMiCE data streams (including the real time position estimation algorithms use for the cMiCE detectors) as well as compatibility for eventual use of the cards within the bore of a 3T magnet. The challenge in board layout is to make the many connections between the FPGA and the board components without introducing time skews for bits in parallel data paths nor restrict the bandwidth of data paths while keeping the board compact.

To that end, a considerable effort has gone into the final design of the board during this past year. To support eventual use of the boards with PET insert designs we have for MRI systems, the board width was fixed at 104 mm. The current printed circuit board (PCB) layout has a length of 216 mm. The initial board layout required 20 layers and did not take into account many manufacturing issues. For example, there are restrictions on the number of different layers can be connected with vias from any one layer due to the manufacturing process and avoiding potential areas of failure over time and layouts that allow the board to be built up symmetrically to avoid wrapping during fabrication. It became clear that the schematic layout (in particular the pin assignments for the FPGA) had to be done iteratively with the PCB layout. Such a process allows for minimization of path lengths and reduces the number of required layers in part by reducing the number of traces that need to cross over each other. Part of the process is a measurement of the trace lengths and calculation of both time skew and bandwidth capacity (which is also driven by the trace size) to assure that the performance targets for the board can be maintained. For example, each serial ADC integrated circuit contains eight discrete ADCs, each digitizing at a rates up to 70 MHz from a common clock. Each IC then connects to the FPGA with eight serial data lines synchronized to a common clock. The data

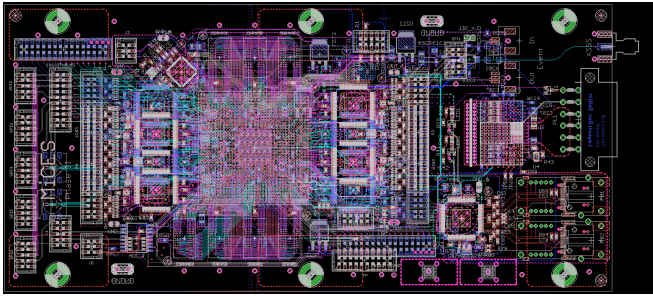rate on each output serial line when digitizing at 70 MHz is 840 mbps.

Figure 4: "X-Ray" view of the layout of the revsion 1 ABN board. The copper power and ground planes are not shown.
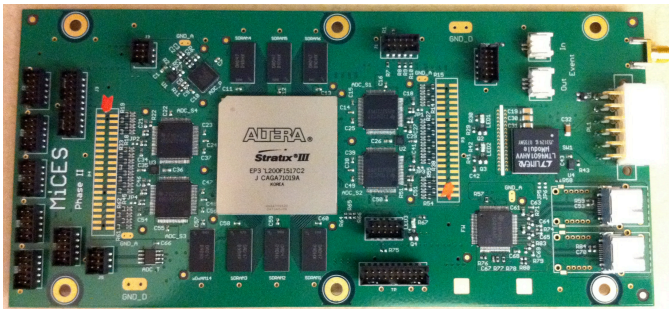

Figure 5: Top view of the revision 1 ABN board. The general layout has cables from the detector modules (up to 64 data channels for energy/position and a 65th channel for a timing signal) coming from the left. Cables to other cards on the right. Cooling will be provided by channels directing air over the board from bottom to top. Cooling fins for the FPGA are not shown.
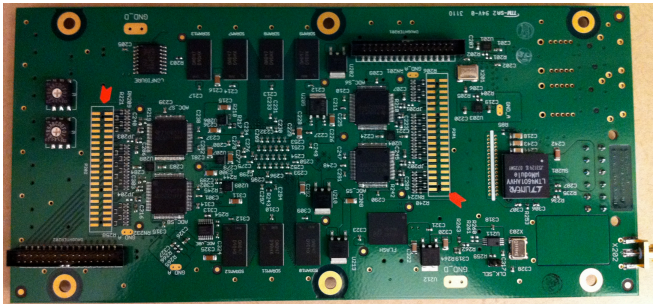

Figure 6: Bottom view of the ABN board.

We investigated using automatic routing vendors for the PCB layouts, but found that the needed optimization of component placement and reduction in board layers (and the correct density of vias interconnecting layers to assure board stability) required manual intervention. As a result, the current design has been done entirely "in-house" by one of our engineers using the Eagle schematic and layout tools (www.cadsoftusa.com). During the process, solid models of the board were produced that allowed confirmation of component spacing, trace clearances, and assured that there was room for the tools used to assemble the board (and possible replacement of components with a ball-grid rework machine).

The result is a 12 layer PCB. Figure 4 is an "x-ray" view of the PCB layout (all layers) from the Eagle software tools and Figures 5 and 6 are images of the first revision of the board that is currently being used for testing and software

development. This board uses an Altera Stratix III FPGA in a F1517 package. Selection of the F1517 package allows a variety of specific Altera FPGAs to be used so that any one board can be configured with the FPGA best suited for the application in terms of capacity and cost. For the current board, we are using a Stratix EP3SL200 which is a high end member of the Stratix III line of FPGAs and has the needed number of phase lock loop (PLL) elements needed to support the ADC I/O requirements to support the cMiCE series of detectors.
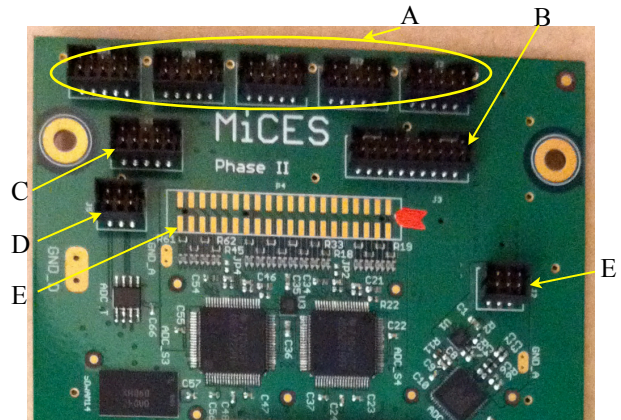

Figure 7: Closeup of right side (top) of the board showing the SPI bus connectors (A), an alternative (one cable) connector for the 5 SPI connectors (B), the two channel logic trigger intpu ©, the temperature sensor connector (D), the parallel ADC connector (E), and one of the four pads for the 64 inputs to the serial ADCs (connector not mounted). In general the inputs are configured as differential pairs.

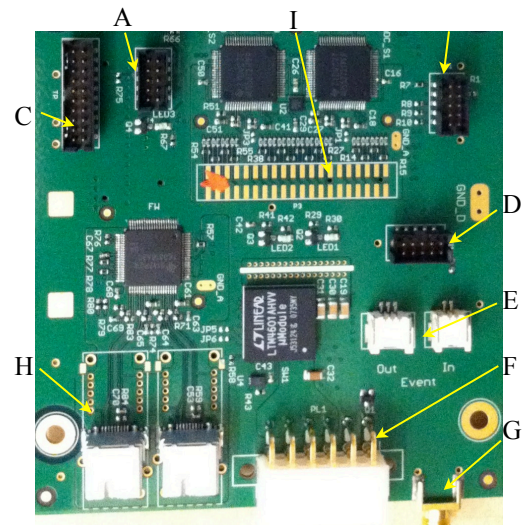Figure 8: Closeup of left side (top) of the board showing the JTAG connectors (A and B), the gneral purpose 10 bit general use connector (C), the SPI bus connector to the master controller (D), the event logic in/out connectors to the master controller (E), power (F), the master clock connector (G), and the FireWire connectors (H) (copper wire connectors are shown mounted). A second set of pads for the serial ADC connector (I).

The left side top (Figure 7) of the card includes five SPI bus connectors (for use by the analog cards, and/or communications to other ANB cards), temperature analog inputs to a dual channel serial ADC, an alternative (one cable) connector for the 5 SPI buses, a connector to the parallel ADC (intended for time pick off signals), and a connector for two channels of logic triggers intended for alternative timing triggers from the analog card. The detector signals are routed to connectors on either side of the serial ADCs (indicated by the pads flagged with red arrows in Figures 5-9; the connectors were not mounted at the time the pictures were taken) and a separate connector is provided on the left side (Figure 7) for the input to the parallel ADC.
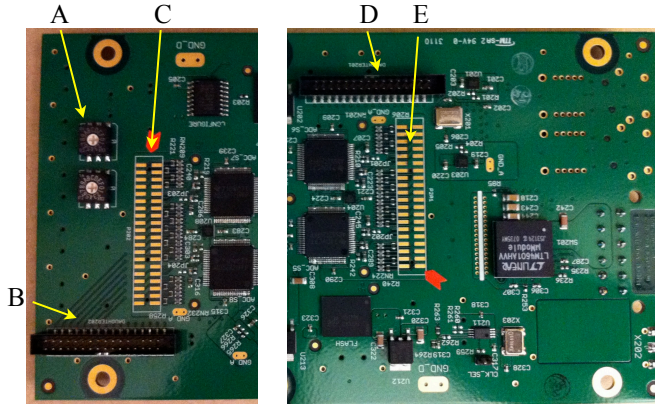

Figure 9: Closeup of bottom side of the board. Left side shows the rotary switches (A), one of the daughter board connectors (B), and a set of pads for one of the four serial ADC connectors (C). Right side shows the second daughter board connector (D) and the last set of seral ADC connector pads (E).

The outgoing FireWire signals, the master clock in, the event present and event accept control lines [10], a SPI bus for command/control from the maser controller, and the power are all on the right side of the card as pictured in Figure 8. When cooled air is required for operation (such as in our MRI insert scanner designs), the air is introduced along the bottom edge of the card and removed along the top edge of the card assuring good flow across the FPGA heat sink and the memories. The current TI FireWire transceiver chip is located at the bottom right of Figure 5. Next to the FireWire transceiver chip are pads for either copper wire FireWire connectors (which are installed in Figure 4) or ethernet optical transceiver/connectors for FireWire over optical or other protocols. There is also a local oscillator that is used to run the card when a master clock is not being supplied to the card (R&D or stand alone operation). The FPGA generates the higher speed clocks needed for the various subsystems.

For future expansion and testing there are two daughter board connectors (16 bits each) on the bottom of the board (Figures 6, 9), a general purpose test/auxiliary signal connector (10 bits) on the front side of the board, a JTAG connector for the FPGA, a JTAG/active serial connector for the load device, two rotary switches connected to the FPGA (e.g., setting board identification data), and several LEDs that monitor power supplies, and FGPA load status.

The cMiCE support requires external memory support for the FPGA and the board is equipped with 380 Mbytes of static random access memory (RAM) for that purpose. An additional 64 Mbytes of static RAM is included for use by the NIOS II embedded processor programmed into the FPGA. For loading the FPGA code and the look up tables used by the cMiCE event estimation algorithms, 512 Mbytes of FLASH RAM is also installed on the board along with an Altera load device (EPCS128). The serial ADCs are currently eight Texas Instruments ADS5272 running at 60 MHz (sending data to the FPGA at 720 mbps per output) providing the 64 channels of event input. The high speed parallel ADC for the timing signal is an Analog Devices AD9211 currently running at 300 MHz.

As of the submission of this conference record in November, 2010, all subsections of the card have been tested and are able to operate at the maximum design speeds. Minor problems were found with some of the manufacturer definition of pin outs on one of the power supplies and the FLASH RAM. In both cases, we were able to correct the problem and continue testing. The minor problems will be corrected in the next revision of the board scheduled for early 2011.

During the design phase, we also allowed for good thermal conductivity from the inner layers of the board and tests have shown that our goals were achieved. However, the good thermal conductivity also presents a challenge for mounting parts on the board, in particular the FPGA, and more extensive tests are being conducted to stress the board thermally to look for any degradation of signal quality due to possible marginal ball-grid connections under the large chips. At this point, it appears that the only precaution required will be to provide a low air flow over a cooling fin on the FPGA when all of the ADCs and memories are in use.

III. DISCUSSION

The first revision of the board has been fabricated and is undergoing tests. Thus far, all the subsystems can be operated at the maximum design speed and only minor problems have been noted. We are in the process of more severe thermal stress testing of the board before fabricating the next revision of the board. The various Verilog code modules we have previously developed are now being assembled into the new system as well as the porting of our previous command and control code used for the Rabbit micro controller to the NOIS II embedded processor in the FPGA. We expect to connect the first test board to a cMiCE detector module in December 2010.

There are several aspects of our design that should be noted. We elected to design a single rather than a set of cards such as we used for our original FireWire data acquisition system or the OpenPet approach to reduce the cost of design and fabrication. The card can be tailored for a wide variety of applications by selection of which components to mount on the board and the selection of the specific FPGA to be used. The Altera F1517 package is used for many different FPGAs in the Stratix II, III, IV, and V product lines. We have not verified that all of these different devices have the same pin assignments for power, ground, and other dedicated signals, but those in the Stratix III line certainly do. Thus, there is a wide range of cost/performance options in deciding what components to actually utilize.

Flexibility is included in many of the I/O options on the board. For example, the connectors A and B in Figure 7 can

also be used as general purpose signal lines - they are not restricted to being defined as SPI buses. In the same way, we can replace the serial ADCs with small ball-grid boards that simply connect the differential inputs directly to the FPGA and can be used, for example, as 64 serial input channels for devices such as the Philips digital SiPM [11].

The variety of topologies that can be supported were discussed in an earlier conference record [10]. What was not apparent in [10] is that the card is not restricted to the use of FireWire. The pinouts on the existing card for the FireWire connectors also supports a range of ethernet connectors - both copper and optical. The transceiver chip would need to be changed (typically with a small board with passive components) in order to connect an ethernet bus approach to the FPGA. For USB or other protocols, the transceiver chip area of the board would either need to be redone or a daughter ball-grid board designed to mount on the pads for the TI FireWire transceiver currently in use. The flexibility is obtained in large part by having the protocol layers in the FPGA rather than in the transceiver chips. That coupled with the flexibility of how the NIOS II soft embedded processor allows the board to support just about any protocol for connection to the host computer.

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