Scott Alan Hauck

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Personal

Born May 4, 1968. US citizenship. Married to Susan Elizabeth Hauck, daughter Lindsey Madison Hauck and son Quinn Cameron Hauck.

Education

Ph.D., Computer Science & Engineering, University of Washington, 1995.
Thesis: *Multi-FPGA Systems*
Advisors: Prof. Gaetano Borriello and Prof. Carl Ebeling.

M.S., Computer Science & Engineering, University of Washington, 1992.

B.S., Electrical Engineering & Computer Science, University of California – Berkeley, 1990.

Research Interests

FPGA Applications, Architectures, Compilers, and CAD Tools; Reconfigurable Computing; FPGAs in High Energy Physics; High-Speed Deep Learning; Computer Engineering Education.

Awards

2015-2020: Gaetano Borriello Professorship for Educational Excellence.

2015, IEEE Fellow, for contributions to Field Programmable Gate Array based systems.

GeekWire Innovation of the Year, 2017, Microsoft Project Catapult.

Top Picks paper: Andrew Putnam, Adrian M. Caulfield, Eric S. Chung, Derek Chiou, Kypros Constantinides, John Demme, Hadi Esmaeilzadeh, Jeremy Fowers, Gopi Prashanth Gopal, Jan Gray, Michael Haselman, Scott Hauck, Stephen Heil, Amir Hormati, Joo-Young Kim, Sitaram Lanka, James Larus, Eric Peterson, Simon Pope, Aaron Smith, Jason Thong, Phillip Yi Xiao, Doug Burger, "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services", *IEEE Micro*, 2015.

FCCM20: Highlights of the First Twenty Years of the IEEE Symposium on Field-Programmable Custom Computing Machines, 2013. 4 of 25 papers in this volume – most of any author, and twice the number of any other author except 1:

S. Hauck, T. W. Fry, M. M. Hosler, J. P. Kao, "The Chimaera Reconfigurable Functional Unit", *IEEE Symposium on FPGAs for Custom Computing Machines*, pp. 87-96, 1997.

S. Hauck, Z. Li, E. J. Schwabe, "Configuration Compression for the Xilinx XC6200 FPGA", *IEEE Symposium on FPGAs for Custom Computing Machines*, pp. 138-146, 1998.

Z. Li, K. Compton, S. Hauck, "Configuration Cache Management Techniques for FPGAs", *IEEE Symposium on FPGAs for Custom Computing Machines*, pp. 22-36, 2000.

P. Banerjee, N. Shenoy, A. Choudhary, S. Hauck, C. Bachmann, M. Haldar, P. Joisha, A. Jones, A. Kanhare, A. Nayak, S. Periyacheri, M. Walkden, D. Zaretsky, "A MATLAB Compiler for Distributed, Heterogeneous, Reconfigurable Computing Systems", *IEEE Symposium on FPGAs for Custom Computing Machines*, pp. 39-48, 2000.

IEEE Symposium on Field-Programmable Custom Computing Machines, Best Paper Award, 2012.
2011 U.W. Dept. of Electrical Engineering Faculty Service Award
2010 University of Washington Distinguished Teaching Award.
2009 College of Engineering Faculty Innovator: Teaching & Learning

Finalist, U.W. Distinguished Teaching Award, 2008.
Best Paper Award, Microelectronic Systems Education Conference, 2007.
Elixent, Inc. S.O.A.P.-Star: Spot On Award Program (employee achievement award), 2006.
Alfred P. Sloan Research Fellow (2001)
U.W. EE Department's Outstanding Research Advisor Award 2001.
Senior Member, ACM (2009)
Senior Member, IEEE (2001)
NSF CAREER award (1999)
1999 IEEE Circuits and Systems Society Transactions on VLSI Systems Best Paper Award
Northwestern University, ECE Department's Best Teacher of 1998/99
June and Donald Brewer Junior Professorship, (Northwestern chair, given up in move to U.W.) 1999-2001
AT&T Bell Laboratories Graduate Fellowship
Berkeley Honors Society
National Merit Finalist
Nominated, U.W. College of Engineering Faculty Innovator for Teaching, 2007, 2008, 2009.
Nominated, U.W. Distinguished Teaching Award, 2004, 2007, 2008, 2009.
Nominated, U.W. College of Engineering Outstanding Faculty Member, 2004.
Nominated, U.W. EE Department's Faculty Service Award, 2004.
Nominated, U.W. EE Department's Outstanding Research Advisor Award 2003, 2004, 2008, 2009.
Nominated, U.W. EE Department's Teaching Award 2001, 2003, 2007.

Awards (to advisees)

College of Engineering Community Innovators Teaching Assistant Innovator Award to Ken Eguro (2008)
College of Engineering Dean's Undergraduate Research Award to Jimmy Xu (2008)
Department of Electrical Engineering Graduate Teaching Award to Ken Eguro (2007)
Yang Research Award to Akshay Sharma (2005), Mike Haselman (2010).
Mary Gates Endowment for Students research training grant to Henry Lee (2003).
Intel Fellowship to Mark Chang (2002)
Lincoln Labs Fellowship to Shawn Phillips (2002)
Cabell Thesis Year Fellowship to Katherine Compton (2002)
U.W. EE Department's Outstanding Research Assistant Award to Mark Chang (2001-2002)
1999 Motorola UPR Best Paper Award (to student Katherine Compton)
National Science Foundation Fellowships to Katherine Compton (1998), Mark Holland (2001), Nathaniel McVicar (2011)
National Science Foundation Fellowship Honorable Mention to Michael Beauchamp (2003 & 2004), Nathaniel McVicar (2010)

Employment

University of Washington, Seattle, WA
9/08 – current Professor.
9/00 – 9/08 Associate Professor.
9/99 – 9/00 Assistant Professor.
Microsoft Research, Redmond, WA.
6/12 – 6/13 Visiting Researcher, eXtreme Computing Group.
7/13 – 3/16 Consultant, eXtreme Computing Group, MSR-T.
Elixent, Ltd, Bristol, England.
8/05 – 6/06 Senior Research Engineer.
Northwestern University, Evanston, IL
10/95 – 9/99 Assistant Professor.
University of Washington, Seattle, WA
3/91 - 9/95 Research Assistant. Investigated multi-FPGA systems, rapid-prototyping, asynchronous design. Developed FPGA architectures. Helped write Orca-C portable parallel programming language.
10/90 - 3/91 Teaching Assistant for Intro. to A.I. & Intro. to Operating Systems
University of California – Berkeley, Berkeley, CA
1/90 - 5/90 Reader. Graded for CS170 – Intro. to Computer Science Theory
1/87 - 5/89 Senior Engineering Aid. Participated in the design and development of the PICASSO user interface for the POSTGRES database project.

I.B.M. – T. J. Watson Research Center, Hawthorne, NY
6/89 - 12/89 Temporary Employee – Co-op. Built a framework and toolkit for a set of X11-based Common Lisp programming tools. System was distributed commercially by Lucid, Inc. as *XLT*.
Bell Communications Research (Bellcore), Morristown, NJ
6/88 - 8/88 Technical Summer Intern. Helped with a Broadband ISDN feasibility study.

Publications

Journal Articles

S. Hauck, S. Burns, G. Borriello, C. Ebeling, "An FPGA For Implementing Asynchronous Circuits", *IEEE Design & Test of Computers*, Vol. 11, No. 3, pp. 60-69, Fall 1994.

S. Hauck, "Asynchronous Design Methodologies: An Overview", *Proceedings of the IEEE*, Vol. 83, No. 1, pp. 69-93, January 1995.

G. Borriello, C. Ebeling, S. Hauck, S. Burns, "The Triptych FPGA Architecture", *IEEE Transactions on VLSI Systems*, Vol. 3, No. 4, pp. 491-501, December 1995.

C. Ebeling, L. McMurchie, S. Hauck, S. Burns, "Placement and Routing Tools for the Triptych FPGA", *IEEE Transactions on VLSI Systems*, Vol. 3, No. 4, pp. 473-482, December 1995.

S. Hauck, G. Borriello, "An Evaluation of Bipartitioning Techniques", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 16, No. 8, pp. 849-866, August 1997.

S. Hauck, G. Borriello, "Pin Assignment for Multi-FPGA Systems", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 16, No. 9, pp. 956-964, September 1997.

S. Hauck, "The Roles of FPGAs in Reprogrammable Systems", *Proceedings of the IEEE*, Vol. 86, No. 4, pp. 615-639, April 1998.

S. Hauck, G. Borriello, C. Ebeling, "Mesh Routing Topologies for Multi-FPGA Systems", *IEEE Transactions on VLSI Systems*, Vol. 6, No. 3, pp. 400-408, September, 1998.

S. Hauck, Z. Li, E. J. Schwabe, "Configuration Compression for the Xilinx XC6200 FPGA", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 8, pp. 1107-1113, August, 1999.

M. Enos, S. Hauck, M. Sarrafzadeh, "Evaluation and Optimization of Replication Algorithms for Logic Bipartitioning", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 9, pp. 1237-1248, September, 1999.

S. Hauck, M. M. Hosler, T. W. Fry, "High Performance Carry Chains for FPGAs", *IEEE Transactions on VLSI Systems*, Vol. 8, No. 2, pp. 138-147, April 2000.

S. Hauck, "FPGA Tools Need Hardware Assistance", *EE Times*, February 16th, 2001.

K. Compton, S. Hauck, "Reconfigurable Computing: A Survey of Systems and Software", *ACM Computing Surveys*, Vol. 34, No. 2, pp. 171-210. June 2002.

K. Compton, Z. Li, J. Cooley, S. Knol, S. Hauck, "Configuration Relocation and Defragmentation for Run-time Reconfigurable Computing", *IEEE Transactions on VLSI Systems*, Vol. 10, No. 3, pp. 209-220, June 2002.

K. Compton, S. Hauck, "Research Focuses on Application-Specific Reconfigurable Blocks", *EE Times*, September 11th, 2002.

S. Hauck, T. W. Fry, M. M. Hosler, J. P. Kao, "The Chimaera Reconfigurable Functional Unit", *IEEE Transactions on VLSI Systems*, Vol. 12, No. 2, pp. 206-217, February 2004.

M. L. Chang, S. Hauck, "Précis: A User-Centric Word-Length Optimization Tool", *IEEE Design & Test of Computers*, Vol. 22, No. 4, pp. 349-361, July-August 2005.

T. Fry, S. Hauck, "SPIHT Image Compression on FPGAs", *IEEE Transactions on Circuits and Systems for Video Technology*, Vol. 15, No. 9, pp. 1138-1147, September 2005.

K. Eguro, S. Hauck, "Resource Allocation for Coarse Grain FPGA Development", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 24, No. 10, pp. 1572-1581, October 2005.

A. Sharma, C. Ebeling, S. Hauck, "PipeRoute: A Pipelining-Aware Router for Reconfigurable Architectures", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 3, pp. 518-532, March 2006.

M. Holland, S. Hauck, "Automatic Creation of Domain-Specific Reconfigurable CPLDs for SoC", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 26, No. 2, pp. 291-295, February 2007.

K. Compton, S. Hauck, "Automatic Design of Area-Efficient Configurable ASIC Cores", *IEEE Transactions on Computers*, Vol. 56, No. 5, pp. 662-672, May 2007.

M. J. Beauchamp, S. Hauck, K. D. Underwood, K. S. Hemmert, "Architectural Modifications to Enhance the Floating-Point Performance of FPGAs", *IEEE Transactions on VLSI Systems*, Vol. 16, No. 2, pp. 177-187, February 2008.

K. Compton, S. Hauck, "Automatic Design of Reconfigurable Domain-Specific Flexible Cores", *IEEE Transactions on VLSI Systems*, Vol 16, No. 5, pp. 493-503, May 2008.

M. Haselman, S. Hauck, "The Future of Integrated Circuits: A Survey of Nano-electronics", *Proceedings of the IEEE*, Vol. 98, No. 1, pp. 11-38, January 2010.

Zhongho Chen, Alvin W.Y. Su, Ming-Ting Sun, Scott Hauck, "Medical imaging process accelerated in FPGA 82x faster than software", *EE Times*, June 21st, 2011.

D. DeWitt, R. S. Miyaoka, X. Li, C. Lockhart, T. K. Lewellen, S. Hauck, "Design of an FPGA based Algorithm for Real-Time Solutions of Statistics-Based Positioning", *IEEE Transactions on Nuclear Science*, vol. 57(1): pp. 2769-2776, February 2010.

N. G. Johnson-Williams, R. S. Miyaoka, X. Li, T. K. Lewellen, S. Hauck, "Design of a Real Time FPGA-based Three Dimensional Positioning Algorithm", *IEEE Transactions on Nuclear Science*, vol. 58(1): pp. 26-33, February 2011

K. Papadimitriou, A. Dollas, S. Hauck, "Performance of Partial Reconfiguration in FPGA Systems: A Survey and a Cost Model", *ACM Transactions on Reconfigurable Technology and Systems*, vol. 4, issue 4, December 2011.

M. D. Haselman, J. Pasko, S. Hauck, T. K. Lewellen, R. S. Miyaoka, "FPGA-Based Pulse Pile-up Correction", *IEEE Transactions on Nuclear Science*, Vol. 59, No. 5, October 2012.

G. Balbi, M. Bindi, S.P. Chen, D. Falchieri, T.Flick, A. Gabrielli, S. Hauck, S.C. Hsu, M. Kretz, A. Kugel, L. Lama, P. Morettini, R. Travaglini, M. Wensing, "The Read-Out Driver ROD card for the Insertable B-layer (IBL) detector of the ATLAS experiment: commissioning and upgrade studies for the Pixel Layers 1 and 2", *Journal of Instrumentation*, Vol. 9, Issue 1, Jan 2014.

T.K. Lewellen, D. DeWitt, R.S. Miyaoka, S. Hauck, "A Building Block for Nuclear Medicine Imaging Systems Data Acquisition", *IEEE Transactions on Nuclear Science*, Vol. 61, No. 1, Feb 2014.

Andrew Putnam, Adrian M. Caulfield, Eric S. Chung, Derek Chiou, Kypros Constantinides, John Demme, Hadi Esmaeilzadeh, Jeremy Fowers, Gopi Prashanth Gopal, Jan Gray, Michael Haselman, Scott Hauck, Stephen Heil, Amir Hormati, Joo-Young Kim, Sitaram Lanka, James Larus, Eric Peterson, Simon Pope, Aaron Smith, Jason Thong, Phillip Yi Xiao, Doug Burger, "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services", *IEEE Micro*, 2015.

Andrew Putnam, Adrian M. Caulfield, Eric S. Chung, Derek Chiou, Kypros Constantinides, John Demme, Hadi Esmaeilzadeh, Jeremy Fowers, Gopi Prashanth Gopal, Jan Gray, Michael Haselman, Scott Hauck, Stephen Heil, Amir Hormati, Joo-Young Kim, Sitaram Lanka, James Larus, Eric Peterson, Simon Pope, Aaron Smith, Jason

Thong, Phillip Yi Xiao, Doug Burger, “A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services”, *Communications of the ACM*, Vol. 59, No. 11, pp 114-122, November 2016.

Aaron Wood, Scott Hauck, “Offset Pipelined Scheduling for Coarse Grain Reconfigurable Architectures”, to appear in *ACM Transactions on Reconfigurable Technology and Systems*, 2017.

Aaron Wood, Scott Hauck, “EveryTime Routing for Offset Pipelined Coarse Grain Reconfigurable Architectures”, to appear in *ACM Transactions on Reconfigurable Technology and Systems*, 2017.

B. Abbott, J. Albert, F. Alberti, M. Alex, G. Alimonti, S. Alkire, P. Allport, S. Altenheiner, L.S. Ancu, E. Anderssen, A. Andreani, A. Andreazza, B. Axen, J. Arguin, M. Backhaus, G. Balbi, J. Ballansat, M. Barbero, G. Barbier, A. Bassalat, R. Bates, P. Baudin, M. Battaglia, T. Beau, R. Beccherle, A. Bell, M. Benoit, A. Bermgan, C. Bertsche, D. Bertsche, J. Bilbao de Mendizabal, F. Bindia, M. Bomben, M. Borri, C. Bortolin, N. Bousson, R.G. Boyd, P. Breugnon, G. Brunia, J. Brossamer, M. Bruschia, P. Buchholz, E. Budun, C. Buttar, F. Cadoux, G. Calderini, L. Caminada, M. Capeans, R. Carney, G. Casse, A. Catinaccio, M. Cavalli-Sforza, M. Cerv, A. Cervellia, C.C. Chau, J. Chauveau, S.P. Chen, M. Chu, M. Ciapetti, V. Cindro, M. Citterioa, A. Clark, M. Cobalab, S. Coellia, J. Collot, O. Crespo-Lopez, G.F. Dalla Betta, C. Daly, G. D’Amenab, N. Dann, V. Dao, G. Darboa, C. DaVia, P. David, S. Debieux, P. Delebecque, F. De Lorenzi, R. de Oliveira, K. Dette, W. Dietsche, B. Di Girolamo, N. Dinu, F. Dittus, D. Diyakov, F. Djama, D. Dobos, P. Donderoab, K. Doonan, J. Dopke, O. Dorholt, S. Dube, D. Dzahini, K. Egorov, O. Ehrmann, K. Einsweiler, S. Elles, M. Elsing, L. Eraud, A. Ereditato, A. Eyring, D. Falchieriab, A. Falou, C. Fausten, A. Favaretoab, Y. Favre, S. Feigl, S. Fernandez Perez, D. Ferrere, J. Fleury, T. Flick, D. Forshaw, D. Fougeron, L. Franconi A. Gabrielliab, R. Gaglione, C. Gallrapp, K.K. Gan, M. Garcia-Sciveres, G. Garianoa, T. Gastaldi, I. Gavrilenko, A. Gaudielloab, N. Geffroy, C. Gemmea, F. Gensolen, M. George, P. Ghislain, N. Giangiacomiab, S. Gibson, M.P. Giordaniab, D. Giugnia, H. Gjersdal, K.W. Glitza, D. Gnani, J. Godlewski, L. Gonella, S. Gonzalez-Sevilla, I. Gorelov, A. Gorišek, C. Gössling, S. Grancagnolo, H. Gray, I. Gregor, P. Grenier, S. Grinstein, A. Gris, V. Gromov, D. Grondin, J. Grosse-Knetter, F. Guescini, E. Guidoab, P. Gutierrez G. Hallewell, N. Hartman, S. Hauck, J. Hasi, A. Hasib, F. Hegner, S. Heidbrink, T. Heim, B. Heinemann, T. Hemperek, N.P. Hessey, M. Hetmánek, R.R. Hinman, M. Hoeferkamp, T. Holmes, J. Hostachy, S.C. Hsu, F. Hügging, C. Husi, G. Iacobucci, I. Ibragimov, J. Idarraga, Y. Ikegami, T. Ince, R. Ishmukhametov, J. M. Izen, Z. Janoška, J. Janssen, L. Jansen, L. Jeanty, F. Jensen, J. Jentzsch, S. Jezequel, J. Joseph, H. Kagan, M. Kagan, M. Karagounis, R. Kass, A. Kastanas, C. Kenney, S. Kersten, P. Kind, M. Klein, R. Klingenberg , R. Kluit, M. Kocian, E. Koffeman, O. Korchak, I. Korolkov, I. Kostyukhina-Visoven, S. Kovalenko, M. Kretz, N. Krieger, H. Krüger, A. Kruth, A. Kugel, W. Kuykendall, A. La Rosa, C. Lai , K. Lantzsch, C. Lapoire, D. Laporte, T. Laria, S. Latorrea, M. Leyton, B. Lindquist, K. Looper, I. Lopez, A. Lounis, Y. Lu, H.J. Lubatti, S. Maeland, A. Maier, U. Mallik, F. Mancaa, B. Mandelli, I. Mandic, D. Marchand, G. Marchiori, M. Marx, N. Massol, P. Mättig, J. Mayer, G. Mc Goldrick, A. Mekkaoui, M. Menouni, J. Menu, C. Meronia, J. Mesa, S. Michal, S. Miglioranziab, M. Mikuž, A. Miucci, K. Mochizuki, M. Monti a, J. Moore, P. Morettinia, A. Morley, J. Moss, D. Muenstermann, P. Murray, K. Nakamura, C. Nellist, D. Nelson, M. Nessi, R. Nisius, M. Nordberg, F. Nuiry, T. Obermann, W. Ockenfels, H. Oidea, M. Oriunno, F. Ould-Saada, C. Padilla, P. Pangaud, S. Parker, G. Pelleriti, H. Pernegger, G. Piacquadio, A. Picazio, D. Pohl , A. Polinia, X. Pons, J. Popule, X. Portell Bueso, K. Potamianos, M. Povoli, D. Puldon, Y. Pylypchenko, A. Quadt, B. Quayle, F. Rarbi, F. Ragusaab, T. Rambure, E. Richards, C. Riegel, B. Ristic, F. Rivière, F. Rizatdinova O. Røhne, C. Rossia, L.P. Rossia, A. Rovania, A. Rozanov, I. Rubinskiy, M.S. Rudolph, A. Rummler, E. Ruscinoa, F. Sabatinia, D. Salek, A. Salzburger, H. Sandaker, M. Sanninoab, B. Sanny, T. Scanlon, J. Schipper, U. Schmidt, B. Schneider, A. Schorlemmer, N. Schroer, P. Schwemling, A. Sciuccati, S. Seidel, A. Seiden, P. Šícho, P. Skubic, M. Sloboda, D.S. Smith, M. Smith, A. Sood, E. Spencer, M. Stramaglia, M. Strauss, S. Stucci, B. Stugu, J. Stupak, N. Styles, D. Su, Y. Takubo, J. Tassan, P. Teng, A. Teixeira, S. Terzo, X. Therry, T. Todorov, M. Tomášek, K. Toms, R. Travaglinia, W. Trischuk, C. Troncon a, G. Troska, S. Tsiskaridze , I. Tsurin, D. Tsybychev, Y. Unno, L. Vacavant, B. Verlaat, E. Vigeolas, M. Vogt, V. Vrba, R. Vuillermet, W. Wagner, W. Walkowiak, R. Wang, S. Watts, M.S. Weber, M. Weber, J. Weingarten, S. Welch, S. Wenig, M. Wensing, N. Wermes, T. Wittig, M. Wittgen, T. Yildizkaya, Y. Yang, W. Yao, Y. Yi, A. Zaman, R. Zaidan, C. Zeitnitz, M. Ziolkowski, V. Zivkovic, A. Zoccoliab, L. Zwalinski, “Production and Integration of the ATLAS Insertable B-Layer”, submitted to *Journal of Instrumentation*, 2018.

Nhan Tran, Javier Duarte, Philip Harris, Scott Hauck, Burt Holzman, Shih-Chieh Hsu, Suffian Khan, Benjamin Kreis, Miaoyuan Liu, Vladimir Loncar, Jennifer Ngadiuba, Kevin Pedro, Brandon Perez, Maurizio Pierini, Dylan Rankin, Sergo Jindariani, Matthew Trahms, Aristeidis Tsaris, Colin Versteeg, Ted W. Way, Dustin Werran, Zhenbin Wu, “FPGA-accelerated machine learning inference as a service for particle physics computing”, *Computing and Software for Big Science*, Vol. 3, No. 13, December 2019.

Krupa, Jeffrey; Lin, Kelvin; Acosta Flechas, Maria; Dinsmore, Jack; Duarte, Javier; Harris, Philip; Hauck, Scott; Hsu, Shih-Chieh; Holzman, Burt; Klijnsma, Thomas; Liu, Mia; Pedro, Kevin; Suaysom, Natchanon; Trahms, Matthew; Tran, Nhan, "GPU coprocessors as a service for deep learning inference in high energy physics", submitted to *Machine Learning: Science and Technology*, 2020.

Patents & Invention Disclosures

S. Hauck, G. Borriello, S. Burns, C. Ebeling, "Field-Programmable Gate Array for Synchronous and Asynchronous Operation", U.S. Patent 5,367,209, issued November 22, 1994.

M. Haselman, R. Miyaoka, T. Lewellen, S. Hauck, "Data Acquisition for Positron Emission Tomography", U.S. Patent 8,003,948 B2, issued August 23, 2011. European Patent filed November 6, 2010.

M. Haselman, R. Miyaoka, T. Lewellen, S. Hauck, "Data Acquisition for Positron Emission Tomography", U.S. Patent 8,309,932 B2, issued November 13, 2012. Continuation of 8,003,948.

K. Eguro, S. Hauck, "Enhancing Timing-Driven FPGA Placement for Pipelined Netlists", *U.S. Provisional Patent Application No. 61/012,728*, December 10, 2007.

T. K. Lewellen, M. Haselman, S. Hauck, UW Ref #8382D, June 2, 2009.

T. K. Lewellen, R. Miyaoka, C. Hayes, S., *Implementation of FPGA pulse processing algorithms for radiation detectors*, Record of Innovation Ref #527 Hauck M. Haselman, L. MacDonald, *MR-PET insert system designs*, Record of Innovation Ref #589, UW Ref #8424D, July 28, 2009.

B. Ylvisaker, C. Ebeling, S. Hauck, *Hyperblock Synthesis for Software Pipelining*, Record of Innovation Ref #726, UW Ref # 8540D, December 8, 2009.

Joo-Young Kim, Jeremy Fowers, Scott Hauck, Douglas Burger, *Scalable High-Bandwidth Architecture for Lossless Compression*, U.S. Patent 9,590,655, issued March 7, 2017.

Scott Hauck, Douglas Burger, *Hardware LZMA Compressor*, U.S. Patent 10,565,182, issued February 18, 2020.

Theses, Books and Book Chapters

J. A. Brzozowski, S. Hauck, C.-J. H. Seger, "Chapter 15: Design of Asynchronous Circuits", in J. A. Brzozowski, C.-J. H. Seger, *Asynchronous Networks*, Springer-Verlag, 1995.

S. Hauck, Multi-FPGA Systems, Ph.D. Thesis, University of Washington, Dept. of CS&E, September, 1995.

A. C. Miguel, R. E. Ladner, E. A. Riskin, S. Hauck, D. K. Barney, A. R. Askew, A. Chang, "Predictive Coding of Hyperspectral Images", in G. Motta, F. Rizzo, J. A. Storer (editors), *Hyperspectral Data Compression*, Springer Science & Business Media, Inc: NY, pp. 197-232, 2006.

S. Hauck, "Field-Programmable Gate Arrays", *McGraw-Hill Encyclopedia of Science & Technology*, 10th edition, 2006.

S. Hauck, "Field-Programmable Gate Arrays", *McGraw-Hill Yearbook of Science & Technology*, 2007, pp. 81-84.

S. Hauck, A. DeHon (editors), *Reconfigurable Computing: The Theory and Practice of FPGA-based Computation*, Morgan Kaufmann/Elsevier, 2008.

B. Ylvisaker, S. Hauck, "Software Engineering for Reconfigurable Computing Systems", *Encyclopedia of Software Engineering*, Taylor & Francis Group, 2010.

Student Theses

M. Enos, *Replication for Logic Partitioning*, Master's Thesis, Northwestern University, Dept. of EECS, 1996.

O. Stone, *A Comparison of ASIC Implementation Alternatives*, Master's Thesis, Northwestern University, Dept. of ECE, 1996.

M. Hosler, *High Performance Carry Chains for FPGAs*, Master's Thesis, Northwestern University, Dept. of ECE, 1997.

G. Gu, *Accelerating Photoshop Applications with Reconfigurable Hardware*, Master's Thesis, Northwestern University, Dept. of ECE, 1999.

M. Chang, *Adaptive Computing in NASA Multi-Spectral Image Processing*, Master's Thesis, Northwestern University, Dept. of ECE, 1999.

K. Compton, *Programming Architectures for Run-Time Reconfigurable Systems*, Master's Thesis, Northwestern University, Dept. of ECE, 1999.

T. Fry, *Hyperspectral Image Compression on Reconfigurable Platforms*, Master's Thesis, University of Washington, Dept. of EE, 2001.

M. Richmond, *A Lemple-Ziv based Configuration Management Architecture for Reconfigurable Computing*, Master's Thesis, University of Washington, Dept. of EE, 2001.

C. Mulpuri, *Runtime and Quality Tradeoffs in FPGA Placement and Routing*, Master's Thesis, Northwestern University, Dept. of ECE, 2001.

S. Phillips, *Automatic Layout of Domain Specific Reconfigurable Subsystems for System-on-a-Chip*, Master's Thesis, Northwestern University, Dept. of ECE, 2001.

A. Sharma, *Development of a Place and Route Tool for the RaPiD Architecture*, Master's Thesis, University of Washington, Dept. of EE, 2001.

M. Holland, *Harnessing FPGAs for Computer Architecture Education*, Master's Thesis, University of Washington, Dept. of EE, 2002.

Z. Li, *Configuration Management Techniques for Reconfigurable Computing*, Ph.D. Thesis, Northwestern University, Dept. of ECE, 2002.

K. Eguro, *RaPiD-AES: Developing an Encryption-Specific FPGA Architecture*, Master's Thesis, University of Washington, Dept. of EE, 2002.

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Javier Duarte, Christian Herwig, Burt Holzman, Sergo Jindariani, Benjamin Kreis, Mia Liu, Ryan Rivera, Nhan Tran, Vladimir Loncar, Jennifer Ngadiuba, Maurizio Pierini, Sioni Summers, Scott Hauck, Shih-Chieh Hsu, Zhenbin Wu, Edward Kreiner, Song Han, Phil Harris, Dylan Rankin, "Low-latency machine learning inference on FPGAs", *NeurIPS Workshop on Machine Learning and the Physical Sciences (ML4PS),* 2019.

Workshop Reports

J. Cong et. al, *Final Report: NSF/NSC International Workshop on Challenges and Opportunities In Giga-Scale Integration For System-On-A-Chip*, Taiwan, August 1999.

Technical Reports

S. Hauck, G. Borriello, C. Ebeling, "Achieving High-Latency, Low-Bandwidth Communication: Logic Emulation Interfaces", *University of Washington, Dept. of CSE Technical Report #95-04-04*, January 1995.

S. Hauck, G. Borriello, C. Ebeling, "Springbok: A Rapid-Prototyping System for Board-Level Designs", 1995.

S. Hauck, A. Agarwal, "Software Technologies for Reconfigurable Systems", *Northwestern University, Dept. of ECE Technical Report*, 1996.

K. Compton, S. Hauck, "Mapping Methods for the Chimaera Reconfigurable Functional Unit", *Northwestern University, Dept. of ECE Technical Report*, 1997.

S. Hauck, S. Knol, "Data Security for Web-based CAD", *Northwestern University, Dept. of ECE Technical Report*, 1998.

S. Hauck, W. D. Wilson, "Runlength Compression Techniques for FPGA Configurations", *Northwestern University, Dept. of ECE Technical Report,* 1998.

Z. A. Ye, N. Shenoy, S. Hauck, P. Banerjee, A. Moshovos, "A C Compiler for a Processor with a Reconfigurable Functional Unit", *Northwestern University, Dept. of ECE Technical Report*, 1999.

Z. A. Ye, A. Moshovos, S. Hauck, N. Shenoy, P. Banerjee, "CHIMAERA: Integrating a Reconfigurable Functional Unit into a High-Performance, Dynamically-Scheduled Superscalar Processor", Technical Report, 1999.

P. Banerjee, A. Choudhary, S. Hauck, N. Shenoy, C. Bachmann, M. Chang, M. Haldar, P. Joisha, A. Jones, A. Kanhare, A. Nayak, S. Periyacheri, M. Walkden, "MATCH: A MATLAB Compiler for Adaptive Computing Systems", 1999.

K. Eguro, S. Hauck, "synFPGA: Application Specific FPGA Synthesis", *Northwestern University, Dept. of ECE Technical Report*, 2000.

K. Compton, J. Cooley, S. Knol, S. Hauck, "Configuration Relocation and Defragmentation for FPGAs", *Northwestern University, Dept. of ECE Technical Report,* 2000.

S. Hauck, Z. Li, "Improved Configuration Prefetch for Single Context Reconfigurable Coprocessors", *Technical Report*, 2000.

T. Owen, S. Hauck, "Arithmetic Compression on SPIHT Encoded Images", *University of Washington, Dept. of EE Technical Report UWEETR-2002-0007*, 2002.

M. Holland, J. Harris, S. Hauck, "Harnessing FPGAs for Computer Architecture Education", *University of Washington, Dept. of EE Technical Report*, 2002.

K. Eguro, S. Hauck, "Decipher: Architecture Development of Reconfigurable Encryption Hardware", *University of Washington, Dept. of EE Technical Report UWEETR-2002-0012*, 2002.

K. Compton, S. Hauck, "Track Placement: Orchestrating Routing Structures to Maximize Routability", *University of Washington, Dept. of EE Technical Report UWEETR-2002-0013*, 2002.

A. Sharma, C. Ebeling, S. Hauck, "PipeRoute: A Pipelining-Aware Router for FPGAs", *University of Washington, Dept. of EE Technical Report UWEETR-2002-0018*, 2002.

Z. Li, S. Hauck, "Don't Care Discovery for FPGA Configuration Compression", 2002.

Z. Li, S. Hauck, "Configuration Prefetching Techniques for Partial Reconfigurable Coprocessor with Relocation and Defragmentation", *Technical Report*, 2003.

Z. Li, K. Compton, S. Hauck, "Configuration Caching Management Techniques for Reconfigurable Computing", *Technical Report*, 2003.

K. Compton, S. Hauck, "Track Placement: Orchestrating Routing Structures to Maximize Routability", Technical Report, 2003.

Z. Li, S. Hauck, "Configuration Compression for Virtex FPGAs", *Technical Report*, 2004.

K, Eguro, S. Hauck, "Issues of Wirelength Cost Models in Routing-Constrained FPGAs", *University of Washington, Dept. of EE Technical Report UWEETR-2004-0006*, 2004.

A. C. Miguel, A. R. Askew, A. Chang, S. Hauck, R. E. Ladner, E. Riskin, "Reduced Complexity Wavelet-Based Predictive Coding of Hyperspectral Images for FPGA Implementation", *Technical Report*, 2004.

A. Sharma, K. Compton, C. Ebeling, S. Hauck, "Exploration of RaPiD-style Pipelined FPGA Interconnects", *Technical Report*, 2004.

S. Phillips, A. Sharma, S. Hauck, "Layout Generation for Domain-Specific FPGAs", Technical Report, 2004.

M. Haselman, M. Beauchamp, A. Wood, S. Hauck, K. Underwood, K. Scott Hemmert, "A Comparison of Floating Point and Logarithmic Number Systems for FPGAs", Technical Report, 2005.

A. Sharma, C. Ebeling, S. Hauck, "Architecture-Adaptive Routability-Driven Placement for FPGAs", *Technical Report*, 2006.

S. Hauck, K. Compton, K. Eguro, M. Holland, S. Phillips, A. Sharma, "Totem: Domain-Specific Reconfigurable Logic", *Technical Report*, 2006.

M. Holland, S. Hauck, "Domain-Specific Reconfigurable PAL/PLA Creation for SoC", *Technical Report*, 2007.

B. Ylvisaker, A. Carroll, S. Friedman, B. Van Essen, C. Ebeling, D. Grossman, S. Hauck, "Macah: A "C-Level" Language for Programming Kernels on Coprocessor Accelerators", *Technical Report*, 2008.

M.D. Haselman, S. Hauck, T.K. Lewellen, R.S. Miyaoka, "Digital Pulse Timing in FPGAs for Positron Emission Tomography", Technical Report, 2008.

K. Eguro, S. Hauck, "Enhancing Routing Heuristics on Pipelined-FPGAs", Technical Report, 2008.

B. Ylvisaker, C. Ebeling, S. Hauck, "Enhanced Loop Flattening for Software Pipelining of Arbitrary Loop Nests", Technical Report, 2010.

Aaron Wood, Adam Knight, Benjamin Ylvisaker, Scott Hauck, “Multi-Kernel Floorplanning for Enhanced CGRAs”, Technical Report UWEETR-2012-0003, 2012.

Marshal Barrett, Scott Hauck, Robert Miyaoka, Tom Lewellen, “Integrating Timing And Positioning Algorithms Onto A Single FPGA Platform For Positron Emission Tomography”, Technical Report, 2012.

Aaron Wood, Scott Hauck, “Offset Pipelined Scheduling, Placement, and Routing for Branching CGRAs”, Technical Report, 2016.

Nathaniel McVicar, Akina Hoshino, Anna La Torre, Thomas A. Reh, Walter L. Ruzzo, Scott Hauck, "FPGA Acceleration of Short Read Alignment," 2017.

Nathaniel McVicar, Akina Hoshino, Anna La Torre, Thomas A. Reh, Walter L. Ruzzo, Scott Hauck, “FPGA Acceleration of Short Read Classification”, 2018.

Grants & Contracts

Funded

National Science Foundation, 6/97-5/99. Scott Hauck, Majid Sarrafzadeh, *Mapping Time Oriented Tools for Logic Emulation*, $219,000 (including matching of $75,000 from AT&T, $25,000 from Northwestern).

National Science Foundation, Research Experiences for Undergraduates, 9/97-8/99. Scott Hauck, $20,000.

Defense Advanced Research Projects Agency, 9/97-8/00. Scott Hauck, Prithviraj Banerjee, Majid Sarrafzadeh, *Architectures, Compilers, and Configuration Management for Mass-Market Adaptive Computing*, $1,981,469.

Defense Advanced Research Projects Agency, 4/98-3/01. Prithviraj Banerjee, Alok Choudhary, Scott Hauck, Nagaraj Shenoy, *A MATLAB Compilation Environment For Adaptive Computing Systems*, $1,855,662.

Xilinx, 9/00-6/01. Scott Hauck, *Compression Techniques for FPGA Configurations*, $40,000.

National Science Foundation, CISE Research Infrastructure Program, 1997-2002. Prithviraj Banerjee, Alok Choudhary, Scott Hauck, D. T. Lee, Majid Sarrafzadeh, Peter Scheuermann, Valerie Taylor, *A Distributed High-Performance Computing Infrastructure*, $906,512.

Motorola, University Partnership in Research Program, 9/97-8/02. Scott Hauck, *Dynamically Reconfigurable Hardware for Digital Signal Processing*, $81,577.

National Aeronautics and Space Administration, 9/00-8/03. Scott Hauck, Prithviraj Banerjee, *MATLAB-Based Adaptive Computing for NASA Image Processing Applications*, $758,358 ($379,938 U.W. + $309,835 Northwestern + $68,585 NASA GSFC).

National Aeronautics and Space Administration, 9/00-8/03. Scott Hauck, Eve Riskin, *Reconfigurable Computing Based Compression for Spaceborne Hyperspectral Images*, $642,043 ($573,458 U.W. + $68,585 NASA GSFC).

National Science Foundation, CAREER Program, 9/99-8/04. Scott Hauck, *Logic Emulation Infrastructure for Research and Teaching*, $240,000.

National Science Foundation, 9/00-8/05. David Allstot, Jeff Bilmes, Chris Diorio, Carl Ebeling, Scott Hauck, Hui Liu, Sumit Roy, Carl Sechen, Richard Shi, Mani Soma, *Heterogeneous System Integration in System-on-a-Chip Designs*, $4,113,001 (incl. $113,001 Supplement).

Sloan Research Fellowship, 9/01-8/05. Scott Hauck, $40,000.

Altera Inc, 11/04 – 8/05. Scott Hauck, *Architecture Adaptive Routability-Driven Placement for FPGAs*, $26,623.

Sandia National Labs, 1/04-12/05. Scott Hauck, *Reconfigurable Hardware for Floating-Point Computations*, $130,957.

U.W. – Royalty Research Fund, 1/05 – 1/06. Scott Hauck, *Self-Assembled Nano-FPGAs*, $26,212.

National Science Foundation, CISE-RI Program, 9/01-8/07. Scott Hauck, David Allstot, Carl Ebeling, Carl Sechen, Mani Soma, Scott Dunham, Richard Shi, Greg Zick, *An Infrastructure for Integrated Systems Education and Innovation*, $1,458,565 ($872,490 NSF + $295,075 Sun + $291,000 UW Cost Sharing).

Altera Inc, 1/07 – 12/07. Scott Hauck, Thomas K. Lewellen, *FPGA-Based Electronics for Advanced PET and PET/MRI Scanners*, $20,000.

National Science Foundation, 11/04-10/08. Scott Hauck, *Achieving High-Performance Reconfigurable Computing in Commodity Devices*, $325,000. Grant #CCF0426147.

Microsoft, 2009. Cascadia Sponsorship, $1,000.

Washington Technology Center/Impulse Accelerated Technologies, 7/08 – 6/09. Scott Hauck, Adam Alession, *Application and Benchmarking of Impulse C Technology to Medical Imaging Tasks*, $120,000.

Department of Energy, 9/06 – 8/09. Carl Ebeling, Scott Hauck, *A High-Performance, Low-Power Configurable Fabric for Embedded Applications*, $730,000. Grant #DE-FG52-06NA27507.

Department of Energy, 11/08 – 10/10. Robert Miyaoka, Thomas K. Lewellen, Scott Hauck, William Hunter, *A High Resolution Monolithic Crystal, DOI, MR Compatible, PET Detector*, $606,314. Grant #DE-FG02-08ER64676.

National Institutes of Health, 2006-2011. Thomas K. Lewellen, Robert S. Miyaoka, Paul E. Kinahan, Marie Janes, Scott A. Hauck, *High Resolution Detectors for Oncology Applications*, $1,895,000 ($1,250,000 direct + $645,000 indirect). Grant #R01 EB002117.

Washington Technology Center/Pico Computing, 7/10 – 6/11. Scott Hauck, Carl Ebeling, Walter Ruzzo, *Acceleration of Genomics Algorithms on Pico Computing Boards*, $120,000. WTC Grant #63-9229

Cypress, 9/10 – 6/11. Scott Hauck, *Placement for Highly Constrained Architectures*, $20,000.

National Science Foundation, 10/07 – 9/11. Carl Ebeling, Scott Hauck, *Tools for Exploring Low-power, High-performance Reconfigurable Computing Architectures*, $379,105. Grant #CCF-0702621.

Zecotek Medical Systems, 3/06 – 6/12. Thomas K. Lewellen, Robert S. Miyaoka, Paul E. Kinahan, Scott A. Hauck, Marie Janes, *High Resolution Positron Emission Tomograph Detector and Electronics Development*, $2,368,222.

Pico Computing, 9/11 – 6/12. Scott Hauck, Larry Ruzzo, Carl Ebeling, *FPGA-based Acceleration of Genomics Applications*, $35,000.

NIH R01 7/09 - 6/13. Robert Miyaoka, Tom Lewellen, Larry MacDonald, Nathan Johnson-Williams, *A Scalable, Monolithic, DOI, TOF, MR Compatible, PET Detector*, $2,236,475.

NSF, 7/11-8/15. Scott Hauck, Carl Ebeling, *SHF: Small: CGRAs – Control and Architecture for Next-Generation FPGAs*, $450,000. Grant #CCF-1116248

NIH RO1, 10/10-9/14. Tom Lewellen, Robert Miyaoka, Scott Hauck, Brian Otis, William Hunter, *High Resolution PET Detectors for Oncology Applications*, $1,404,000 ($900,000 direct + ~$504,000 indirect).

NSF, 1/20-12/21. Phillip Harris, Eliu Huerta Escudero, Song Han, Scott Hauck, Shih-Cheih Hsu, Erotokritos Katsavounidis, Volodymyr V. Kindratenko, Mark S. Neubauer, Zhizhen Zhao, *Collaborative Research: Advancing Science with Accelerated Machine Learning*, $1,800,000.

Donations

Funded

NSF/MOSIS, Donation of integrated circuit fabrication services for educational use, 1998, $5,610.

Tektronix, Dollar match on oscilloscope, 2000, $4,439.

Sun, Dollar match on ultra 5's, 2000, $2,500.

Cypress Semiconductor, Donation of PSOC systems, 2010, $249.

Xilinx, Donation of FPGA boards and mapping software, 1996, $28,050; 1997, $5,925; 1998, $5,725; 2000, $41,948; 2002, $3,990; 2005, $700; 2010, $1,749; 2012, $999; 2014, $2,198; 2015, $1099.

Intel/Altera, Donation of FPGA mapping software, chips, and boards, 2006, $28,220; 2007, $45,780; 2008, $311,800; 2009, $5,995; 2010, $41,508; 2011, $20,756; 2012, $106,674; 2014, $29,700; 2015, $48,600; 2019, $169.73.

F5 Networks, Donations for support of undergraduate research in FPGAs, 2019, $20,000.

Professional Activities

Conference & Journal Organization

Member, FPGA Hall of Fame Committee, 2017.

Member, Best Paper Committee, ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 2014.

Associate Editor, International Journal of Reconfigurable Computing (IJRC), 2007 – 2012.

Member, Panel of Experts, FCCM20: Highlights of the International Symposium on Field-Programmable Custom-Computing Machines, 2013.

Member, Panel of Experts, FPGA20: Highlights of the International Symposium on Field-Programmable Gate Arrays, 2012.

Guest Editor (with Toomas Plaks and others), ACM Transactions on Embedded Computing Systems, special issue on Configurable Computing: Configuring Algorithms, Processes, and Architecture, 2008.

Co-organizer, Cascadia Workshop on FPGAs, 2007, 2009, 2011.

Guest Editor (with Miriam Leeser and Russ Tessier), EURASIP Journal of Embedded Systems, special issue on Field-Programmable Gate Arrays in Embedded Systems, 2006.

Organizer, UBC/UW Workshop on FPGAs, 2005.

Associate Editor, IEEE Transactions on VLSI Systems, 1999 - 2001.

Program Chair, ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 2000.

General Chair, ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 2001.

Finance Chair, ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 2002.

Publicity Chair, ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 1997-1999.

Steering Committee, ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 2000-present.

Topic Chair, Reconfigurable Architectures, International Workshop on Field Programmable Logic and Applications, 2008.

Sub-TPC Chair, Design Automation Conference, 2004.

Program Committee Memberships

ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 1997-2003, 2009-2014.
IEEE Symposium on FPGAs for Custom Computing Machines (FCCM), 1997-2014.
IEEE Microelectronic Systems Education Conference (Bi-annual), 2003, 2005, 2007, 2009, 2011, 2017.
International Workshop on Field Programmable Logic and Applications, 2000, 2002-2005, 2007 – 2011
IEEE International Conference on Field-Programmable Technology (FPT), 2002-2004, 2009
Reconfigurable Architectures Workshop (RAW), 2009
Reconfigurable Computing and FPGA conference (Reconfig), 2004, 2005, 2008, 2009, 2010
Design Automation Conference, 2003 – 2004

International Conference on Engineering of Reconfigurable Systems and Algorithms, 2004
Workshop on Software Support for Reconfigurable Systems (ERSA), 2003
Advanced Research in VLSI 2001
CORE-2000 - Reconfigurable Computing Workshop 2000
Great Lakes Symposium on VLSI, 1997

Keynotes, Panels, Tutorials

Full Day Tutorial Organizer and Presenter, "Reconfigurable Systems: Logic Emulation, Custom Computing, and Beyond", Design Automation Conference, 1997.

Keynote Speaker, "The Future of Reconfigurable Systems", 5th Canadian Conference on Field Programmable Devices, Montreal, June 1998.

Panel Organizer and Moderator, "FPGAs in the Era of System-on-a-Chip", International Symposium on Field Programmable Gate Arrays, 1999.

Panel Member, "Architectures, Technologies and Design Methodologies for 2005 and Beyond", Military and Aerospace Applications of Programmable Logic Devices International Conference, 1999.

Panel Member, "Is Marriage in the Cards for Programmable Logic, Microprocessors and ASICs?", ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 2001.

Bing & FPGAs – Introduction to Catapult, Microsoft Research, January 16 – 18, 2013.

Introduction to FPGA Programming for Software Developers, Microsoft, March 28 – June 1, 2016.

Session Chair, Participant

Session Chair, ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 1997, 1998, 2002, 2005, 2009, 2011; IEEE Symposium on FPGAs for Custom Computing Machines, 1997-2000, 2002 – 2005, 2007; International Symposium on Field-Programmable Logic, 2004.

Session Organizer, DAC 2003 - 2004.

Group Discussion Leader & Presenter, "Reconfigurable Device Architectures", Configurable Computing Workshop, Hewlett-Packard Labs, Bristol, England, 1998.

Participant, National Science Foundation Workshop on Research Directions for Next-Generation Systems Design and Integration, Seattle, WA, June 1999; NSF/NSC Joint Workshop on Challenges and Opportunities In Giga-Scale Integration for System-On-A-Chip, Taiwan, August 1999.

Reviewing

Reviewer, Proceedings of the IEEE, IEEE Transactions on Computers, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on VLSI Systems, IEEE Design & Test of Computers, ACM Transactions on Reconfigurable Technology and Systems, Distributed Computing, NSF, ACM Transactions on Design Automation of Electronic Systems, Microelectronic Systems Education Conference, Design Automation Conference, Journal of VLSI Signal Processing Systems, International Symposium on Computer Architecture, IEEE Journal of Solid-State Circuits, U.W. RRF Program, Natural Sciences and Engineering Research Council of Canada, International Symposium on Microarchitecture, Journal of Signal Processing Systems, South Carolina DEPSCoR, Journal of Systems Architecture.

External Ph.D. Examiner, Mohammed Khalid, University of Toronto, 1998; Joerg Ritter, Martin-Luther-Universität, 2002; Benjamin Levine, CMU, 2004; Julien Lamoureux, University of British Columbia, 2007; David Grant, University of British Columbia, 2011.

Miscellaneous

Honorable Judge, 2018 InnovateFPGA Grand Final.

Evaluator and author of two introductions, FPGA'20: The best papers from the ACM Symposium on FPGAs, 2011.

Selection committee, SIGDA Outstanding New Faculty Award, 2011.

NSF grant review panel, 2010.

Senior Member, ACM; Senior Member, IEEE.

Judge, Hamilton International Middle School Science Fair, 2012.

Judge, Seattle Public Schools Middle School Science Fair, 2001, 2005.

IEEE Admission and Advancement Panel, November 15th, 2003.

Consulting

Motorola, Inc. Technology evaluation, October 1997.

Lyon & Lyon, Orrick/Quickturn, Inc. Expert Witness, August 2000 – February 2003. *Mentor Graphics Corporation vs. Quickturn Design Systems, Inc. and Cadence Design Systems, Inc.*, U.S. District Court for the Northern District of California, Case No. C-00-03291 SI. March 2003 – September 2003. *Quickturn Design Systems, Inc. vs. Mentor Graphics Corporation and M2000*, 3rd Chamber, 2nd Section, of the Civil Court of Paris, France, Roll No. 98/21148.

Data Transit Corp. Expert Witness, May 2003 – June 2003. *I-Tech Corp. vs. Data Transit Corp, The Epoch Group, Inc., and Innotec Design, Inc.*, United States District Court, District of Minnesota, Civil Action No. 02-CV2765 (RHK/AJB).

Berkeley Law and Technology Group, LLC. Technology evaluation, July 2006 – October 2006.

Invention Law Group, PLLC. Technology evaluation, November 2006 – February 2008.

Davis, Rothwell, Earle & Xochihua, PC, in collaboration with Mersereau Shannon LLP. Expert Witness, August 2011 – April 2012. *Morris vs. Evans & Zusman et. Al.*, U.S. District Court for the District of Oregon.

Orrick/Synopsys, Inc. Expert Witness, April 1, 2013 – June 2018. *Mentor Graphics Corporation vs. Synopsys, Inc.* United States District Court, District of Oregon, Portland Division, Case No. 3:10-CV-954-MO; 3:12-CV-1500-MO; 3:13-CV-579-MO.

Sidley Austin/Microsoft. Expert Witness, March 27, 2018 – Ongoing. *SRC Labs and Saint Regis Mohawk Tribe vs. Microsoft, Inc.*

Invited Presentations

Note: Does not include talks associated with conference presentations.

"An FPGA for Asynchronous Circuits", U. of British Columbia, October 25, 1993.

"Multi-FPGA Systems", Northwestern University, February 1995; Cornell University, March 1995; AT&T Bell Labs, March 1995; IBM – T. J. Watson Research Center, March 1995; University of California - Davis, March 1995; Yale University, April 1995; University of Illinois Urbana-Champaign, April 1995, Xilinx, Inc., April 1995; ARPA VLSI Contractors Meeting, April 1995; HP Inc., Boulder, May 1995; HP Labs, Bristol, England, August 21, 1995; UC Berkeley, February 14, 1996.

"An Introduction to Architectures, Compilers, and Configuration Management for Mass-Market Adaptive Computing", DARPA ACS PI Meeting, November 1997.

"Triptych, Montage, Chimaera: Advanced FPGA Technologies", Quicklogic Inc., November 10, 1997.

"Configuration Memory Management for Adaptive Computing Systems", U. Illinois Chicago, January 23, 1998; U. Washington, January 30, 1998; UC Berkeley, April 17, 1998; Carnegie Mellon U., October 12, 1998; University of Toronto, December 11, 1998.

"Lessons Learned", DARPA ACS PI Meeting, April 1998.

"FPGAs @ Northwestern", Motorola, April 30, 1998; ECE Advisory Board, May 10, 1998.

Keynote Address, "The Future of Reconfigurable Systems", 5th Canadian Conference on Field Programmable Devices, Montreal, June 1998.

"The Future of Reconfigurable Systems", Carnegie Mellon U., October 14, 1998.

"Reconfiguration Architectures for Adaptive Computing Systems", University of Washington, January 29,1999.

"The Roles of Reconfigurable Logic in Systems-on-a-Chip", Motorola, April 27, 1999.

"Teaching Engineering Concepts", ECE Excellence in Teaching Seminar, Northwestern University, May 28, 1999.

"Reconfigurable Architectures, Applications, and CAD", Graduate Research Seminar, Dept. of EE, University of Washington, October 15, 1999; Electrical Engineering Research Day, University of Washington, October 22, 1999. IEEE Brown Bag Lunch, University of Washington, October 27, 1999, Graduate Student Recruiting Day, University of Washington, March 6 & March 31, 2000.

"Panel: Research on the Internet and at the EE/CSE Interface", Electrical Engineering Research Day, University of Washington, October 22, 1999.

"Architectures, Compilers, and Configuration Management for Mass-Market Adaptive Computing", DARPA Program Review, April 3, 2000.

"Overview of the Chimaera Project", DARPA PI Meeting, May 22, 2000.

"Research in Reconfigurable Systems", U.W. Dept of EE Workshop for Korean Technology Visitors, July 18, 2000.

"The Chimaera Project", ST Microelectronics, August 29, 2000.

"FPGA Configuration Management in the Chimaera Project", DARPA PI Meeting, October 10, 2000.

"Totem: Domain-Specific Reconfigurable Subsystems for System-on-a-Chip", Motorola Corporate Research, July 31, 2001. Quicksilver Inc., November 30, 2001.

"Variable Precision Analysis Tools", NASA Goddard Teleconference, October 31st, 2001.

"Reconfigurable Computing Based Compression for Hyperspectral Images", NASA Goddard Teleconference, October 31st, 2001.

"Precis: Variable Precision Analysis for FPGA-based Implementations", NASA Goddard Teleconference, April 17th, 2002.

"Extending Reconfigurable Computing Based Compression to Unequal Loss Protection", NASA Goddard Teleconference, April 17th, 2002.

"An Infrastructure for Integrated Systems Education and Innovation", NSF CISE/EIA RIA and MII PI's Workshop, July 13th, 2002.

"Enhanced FPGA-Based Hyperspectral Compression" NASA Goddard Site Review, August 21st, 2002.

"Totem: Domain-specific FPGA Generation", Washington University, Dept. of CSE, October 11th, 2002.

"Compression on FPGAs", Rapid Seminar, 2003.

"Totem: Domain-Specific FPGA Synthesis", NSF ITR Site Visit, July 24th, 2003.

"Welcome", EE Undergraduate Orientation, September 25th, 2003.

"The Time Management Freak Show", ADVANCE Lunch, November 21st, 2003.

"Electrical Engineering" NSBE Department Panel, May 18th, 2004.

"Graduate School: Why & How", U.W. – EE Undergraduates Grad School Panel, May 27th, 2004.

"Variable Precision Analysis for FPGA Synthesis", Sandia National Labs, July 13th, 2004.

"Totem, The Rest of the Story…", University of British Columbia, September 17th, 2004.

Akshay Sharma, Scott Hauck, "Architecture Adaptive A* Techniques for FPGA Routing", *UW/UBC Workshop on FPGAs*, 2005.

Mike Haselman, Scott Hauck, "A Comparison of Floating Point and Logarithmic Number Systems on a FPGA", *UW/UBC Workshop on FPGAs*, 2005.

Ken Eguro, Scott Hauck, "Architecture-Adaptive Range Limit Windowing for Simulated Annealing FPGA Placement", *UW/UBC Workshop on FPGAs*, 2005.

Mark Holland, Scott Hauck, "Automatic Creation of Domain-Specific CPLDs for System-on-a-Chip", *UW/UBC Workshop on FPGAs*, 2005.

"Hyperspectral Image Processing on FPGAs", UW CSE Configurable Computing Seminar, 2006.

Ken Eguro, Scott Hauck, "Pipelining Commodity Reconfigurable Devices", *UW/UBC Workshop on FPGAs*, 2006.

Mike Haselman, Scott Hauck, "An FPGA-Based PET Scanner", *UW/UBC Workshop on FPGAs*, 2006.

"The Time Management Freak Show", ADVANCE Lunch, March 2nd, 2007.

"Research in the ACME Lab", CSE Grad Student Visit Day, 2007.

"Reconfigurable Logic @ U.W.", Microsoft Research, 2007.

Mike Haselman, Scott Hauck, Tom Lewellen, Robert Miyaoka, "FPGA-Based Data Acquisition System for a PET Scanner", *Cascadia Workshop on FPGAs*, 2007.

Ben Ylvisaker, Scott Hauck, "Macah: Simplifying the Programming of Kernel Accelerators with Judicious Automation", *Cascadia Workshop on FPGAs*, 2007.

Brian Van Essen, Scott Hauck, "Molecular Dynamics Simulation for Hybrid Micro-Parallel Systems", *Cascadia Workshop on FPGAs*, 2007.

Ken Eguro, Scott Hauck, "Pipeline and Retiming-Aware Placement", *Cascadia Workshop on FPGAs*, 2007.

Allan Carroll, Stephen Friedman, Robin Panda, Brian Van Essen, Aaron Wood, Benjamin Ylvisaker, Carl Ebeling, Scott Hauck, "Designing a Coarse-grained Reconfigurable Architecture for Performance & Power Efficiency", *U.W. Dept. of CSE Affiliates*, 2007.

"Mosaic: High-Performance, Low-Power Configurable Fabrics for Embedded Applications", Department of Energy Site Visit, December 11th 2007.

"FPGAs for Tomography?", U.W. Dept. of Radiology Seminar, March 27th 2008.

"Mosaic: CAD Tools and Architectures for Coarse-Grained Reconfigurable Arrays", Lawrence Livermore National Labs, August 31st, 2008.

Ken Eguro, Scott Hauck, "Incremental Timing Analysis for FPGA Placement", *Cascadia Workshop on FPGAs*, 2008.

Brian Van Essen, Allan Carroll, Ken Eguro, Stephen Friedman, Robin Panda, Aaron Wood, Benjamin Ylvisaker, Jon Cohen, Maya Gokhale, Carl Ebeling, Scott Hauck, "Mosaic: High-Performance, Low-Power Configurable Fabrics for Embedded Applications", *Cascadia Workshop on FPGAs*, 2008.

Michael Haselman, Don DeWitt, Scott Hauck, Robert Miyaoka, and Thomas Lewellen, "An FPGA-Based Data Acquisition and Pulse Processing System for Positron Emission Tomography", *Cascadia Workshop on FPGAs*, 2008.

Ben Ylvisaker, Carl Ebeling, Brian Grossman, Scott Hauck, "Architectural Adaptation in Macah", *Cascadia Workshop on FPGAs*, 2008.

Stephen Friedman, Allan Carroll, Robin Panda, Brian Van Essen, Aaron Wood, Benjamin Ylvisaker, Carl Ebeling, Scott Hauck, "Mosaic: Coarse-grained Reconfigurable Architecture Exploration", U.W. Dept. of CSE Affiliates, 2008.

"The Time Management Freak Show", ADVANCE Time Management Workshop, March 5, 2009.

Michael Haselman, Nathan Johnson-Williams, Chad Jerde, Maria Kim, Scott Hauck, Robert Miyaoka, Thomas Lewellen, "FPGAs vs. MPPAs for Positron Emission Tomography Pulse Processing", *Cascadia Workshop on FPGAs,* 2009.

Nikhil Subramanian, Jimmy Xu, Scott Hauck, Adam Alessio, "A C-to-FPGA Solution for Accelerating Tomographic Reconstruction", *Cascadia Workshop on FPGAs,* 2009.

Brian Van Essen, Aaron Wood, Allan Carroll, Stephen Friedman, Robin Panda, Benjamin Ylvisaker, Carl Ebeling, Scott Hauck, "Static versus Scheduled Interconnect in Coarse-Grained Reconfigurable Arrays", *Cascadia Workshop on FPGAs,* 2009.

Stephen Friedman, Robin Panda, Benjamin Ylvisaker, Scott Hauck, Carl Ebeling, "Predicate Aware CGRA Mapping - Sharing for Mutually Exclusive Operations", *Cascadia Workshop on FPGAs,* 2009.

Nathan Johnson-Williams, Robert Miyaoka, Xiaoli Li, Tom K. Lewellen, Scott Hauck, "Design of a real-time, FPGA-based 3-dimensional positioning algorithm", Imaging Research Laboratory Scientific Retreat, U.W. Dept. of Radiology, September 24, 2009.

"Graduate School: Why & How", U.W. – EE Undergraduates Grad School Panel, November 23rd, 2009.

ENGR 498b, "What are Graduate Programs Looking For?", January 27th, 2010.

Michael Haselman, Scott Hauck, Thomas Lewellen, Robert Miyaoka, Wendy McDougald "An FPGA-based Pulse Pileup Correction for Positron Emission Tomography", *Cascadia Workshop on FPGAs,* 2010.

Ben Ylvisaker, Carl Ebeling, Scott Hauck, "Enhanced Loop Flattening for Software Pipelining of Arbitrary Loop Nests", *Cascadia Workshop on FPGAs,* 2010.

Brian Van Essen, Robin Panda, Aaron Wood, Carl Ebeling, Scott Hauck, "Managing short-lived and long-lived values in Coarse-Grained Reconfigurable Arrays", *Cascadia Workshop on FPGAs,* 2010.

Robin Panda, Jimmy Xu, Scott Hauck, "Software Managed Distributed Memories in MPPAs", *Cascadia Workshop on FPGAs,* 2010.

Scott Hauck, 'Research as a Team Sport", ADVANCE Collaboration Workshop, March 2, 2011.

Scott Hauck, Higher Education Committee of the State of Washington House of Representatives, April 13, 2011.

Andrew Price, Scott Hauck, Joseph Skudlarek, "Practical Placement for Highly Constrained Heterogenous Architectures", *Cascadia Workshop on FPGAs,* 2011.

Elliott Brossard, Carl Ebeling, Scott Hauck, "A Threaded Object Model for Programmable Configurable Computers", *Cascadia Workshop on FPGAs,* 2011.

Corey Olson, Carl Ebeling, Scott Hauck, Maria Kim, Larry Ruzzo, Cooper Clauson, Boris Kogon, "An FPGA Acceleration of Short Read Human Genome Mapping", *Cascadia Workshop on FPGAs,* 2011.

Nathaniel McVicar, Scott Hauck, "VLIW Compiling for Non-Processor CGRA Clusters", *Cascadia Workshop on FPGAs,* 2011.

Robin Panda, Scott Hauck, "Dynamic Communication in a Coarse Grained Reconfigurable Array", *Cascadia Workshop on FPGAs,* 2011.

Aaron Wood, Adam Knight, Benjamin Ylvisaker, Scott Hauck, "Multi-kernel Floorplanning for Enhanced CGRAs", *Cascadia Workshop on FPGAs,* 2012.

Nathaniel McVicar, Scott Hauck, "Acceleration of Filters Used in ncRNA Homolog Search", *Cascadia Workshop on FPGAs,* 2012.

Robin Panda, Carl Ebeling, Scott Hauck, “Adding Dataflow-Driven Execution Control to a Coarse-Grained Reconfigurable Array”, *Cascadia Workshop on FPGAs*, 2012.

Scott Hauck “FPGA Acceleration of Short Read DNA Mapping”, Microsoft Research, Sept 6 2012.

Matt Humphrey, Phil Hays, Scott Hauck, David Shih, “Intro to FPGAs”, Microsoft Maker Garage Talk & Tutorial, October 16, 2014.

Joo-Young Kim, Jeremy Fowers, Eric Chung, Scott Hauck, Doug Burger, “A Family of High-Throughput, High Quality Compression Engines on Catapult”, Microsoft Faculty Summit, July, 2015.

Duarte, Holzman, Jindariani, Kreis, Lui, Pedro, Tran, Tsaris, Harris, Rankin, Wu, Neubauer, Khan, Perez, Versteeg, Way, Hauck, Hsu, Trahms, Werran, Loncar, Ngadiuba, Pierini, “FPGA Accelerated Machine Learning Inference for Particle Physics”, Connecting the Dots, 2019.

Committees & Departmental Service

University of Washington (1999-current)

Associate Chair for Education, 2020 – ongoing.

Chair, Department Computing Committee, 2019 – 2020.

IEEE Concentrations Panel, 2018, 2019, 2020.

Chair, Department Fellowship Committee, 2018-2020.

CoE Direct to College Student Placement Process Faculty Review Committee, 2018.

ECE formation guiding committee, 2017-2018.

UW Reviewing Officer, Misconduct, 2018-2020.

IEEE/HKN Casino Night Dealer, 2015, 2018, 2019, 2020.

EE Admissions Committee, 2003, 2012, 2018.

UW University Disciplinary Committee, 2017.

BS-MS Admissions Committee, 2015.

EE Chair Search, 2014.

EE Undergraduate Coordinator, 2003 – 2005.

EE Competitiveness Committee, 2014.

Intel PhD fellowship committee, 2014.

Chair’s Advisory Committee for Merit Reviews, 2008, 2012.

EE Taskforce for Daytime MS Programs, Chair, 2012.

Intel Fellowship selection committee, 2012.

University of Washington, Distinguished Teaching Award Selection Committee, 2011, 2020.

EE, Quals Committee, Yuan-Jyue Chen (Controls, 2011), Vaishnavi Ranganathan (2015), Cindy Liu (2020).

EE Department Promotion & Tenure Committee, 2010 - 2012.

EE Administrator Search Committee, 2010.

Co-Chair, *ExCEL* CSE/EE Faculty Recruiting Committee, 2007 – 2010, 2012 – 2013, 2014-2017.

EE Department Ad Hoc committee on workload policy, 2010.

College of Engineering, Community of Innovators Award Selection Committee, 2010.

EE Ad-Hoc Committee on EE Promotion Guidelines., 2010.

Google Fellowship selection committee, 2010.

EE Graduate Fellowship review committee, 2009.

EE Undergraduate Scholarship Committee, 2002, 2009.

EE Undergraduate Admissions Appeals Committee, 2009.

HKN Poker Night Dealer, 2009, 2010, 2011, 2012.

VLSI and Embedded Systems Curriculum Chair, 2007 – 2008.

EE Admissions Committee, Committee Chair, 2003 – 2005, 2008.

EE Merit Review Committee, Chair of Assistant/Lecturer Subcommittee, 2008.

EE Curriculum Committee, 2003 – 2005, 2007 - 2008.

College Council on Educational Policy, 2007.

EE Server and Space Task Force, 2007.

Intel Fellowship review committee, 2007, 2008.

College Council, 2006.

UW Faculty Senate, 2004 – 2005.

EE Chair Search, 2003 – 2004, 2004 - 2005.

EE Faculty Advisory Board, 2000 - 2005.

College of Engineering Accreditation and Continuous Improvement (ACI) Committee, 2003 - 2005.

University of Washington, Commencement Marshall, 2004, 2007, 2008, 2009, 2010, 2011.

EE Outstanding Staff Awards Committee, 2004.

EE Undergraduate Scholarship Committee, Committee Chair, 2004 – 2005.

Chair, EE Ad Hoc Committee on Capstone courses, Committee Chair, 2003-2004.

EE Undergraduate Curriculum Construction Committee, 2002-2003.

EE Undergraduate Graduation Announcer, 2003 – 2004, 2007.

EE Computing Advisory Committee Chair, 2000-2002.

EE Computing Advisory Committee, 1999-2002.

Undergrad seminar, *Intro to "Digital"*, Oct 23rd, 2002; May 21st, 2003.

Civil Engineering Department Chair Search, 2001.

EE Strategic Planning Committee, 1999-2000.

Merit review committee, Sathe (2017, Chair), Arabashi (2017), Seelig (2018, Chair).

Promotion and Tenure Committee, Jim Peckol (Principal Lecturer, 2012), Georg Seelig (Assoc Professor, 2014), Matt Reynolds (special, 2014), Chair: Eric Klavins (Professor, 2015), Josh Smith (Professor, 2016), Shwetak Patel (Professor, 2016).

Promotion and Tenure Review Committee, Brian Otis (2010), Shwetak Patel (2012), Jim Peckol (Chair, 2012).

Faculty Review Committee for Progress Toward Promotion, Jacob Rosen (2002), Katrin Kirchoff (2003, 2004), Mark Holl (Chair, 2005), Larry McMurchie (Chair, 2005), Eric Klavins (2005), Brian Otis (2007; Chair, 2008; Chair, 2009), Eric Klavins (Chair, 2010), Shwetak Patel (2010, 2011), Georg Seelig (Chair, 2012).

Graduate School Representative, Supervisory Committee: Scott Martin (ME, 2001 - 2003), Stephen P. Voght (Genetics, 2002 - 2007), Joe Devietti (CSE, 2011 – 2012), Hadi Esmaeilzadeh (CSE, 2012 – 2013), Benjamin Wood (CSE, 2013 – 2014), Irene Zhang (CSE, 2015 – 2017), Antoine Kaufmann (CSE, 2017 – 2018), Eric A. Mullen (CSE, 2018), Nikola Whallon (Physics, 2018), Waylon Brunette (CSE, 2018 – ongoing), Niel Lebeck (CSE, 2019 – 2020), Helgi Sigu (CSE, 2019 – 2020).

Supervisory Committee, Jovanka Ciric (EE 2001), Yoochang Chung (EE 2001-2002), Su Kio (EE 2001-2003), Jian Zhou (EE 2002-2003), Yi Han (EE 2002-2005), Sheng Sun (EE 2003-2006), Nuttorn Jangkrajarng (EE 2003-2006), Song Li (CSE 2004).

Digital Systems Qualifying Exam Chair, Fall 2004, Fall 2007, Spring 2008.

Digital Systems Qualifying Exam Committee, Spring 2000, Fall 2000, Spring 2001, Fall 2002, Spring 2003, Fall 2004, Fall 2006, Fall 2009, Spring 2011, Fall 2012.

Northwestern University (1995-1999)

EECS/ECE Computing Resources Committee, 1995-1998.

ECE Curriculum Committee, 1996-1998.

Graduate Electrical and Computer Engineering Students Society (GECES) Faculty Co-Advisor, 1997-1999.

Safety Committee Alternate Zone Warden, 1997-1998.

ECE Graduate Committee, 1998-1999.

Undergraduate Computer Engineering Program Committee, 1998-1999.

Computer Engineering Program of Study (POS) Committee Chairman, 1998-1999.

Teaching

University of Washington (Numbers are average of questions 1, 3 & 4. All scores are raw, not adjusted, as presented on the web.)

EE 271: Introduction to Digital Circuits and Systems (formerly 371)
- Winter 2003. Q1 4.5, Q3 4.6, Q4 4.7, Ttl 4.6 (88th percentile in department)
- Fall 2004. Q1 4.7, Q3 4.8, Q4 4.8, Ttl 4.8 (96th percentile in department)
- Fall 2006. Q1 4.60, Q3 4.78, Q4 4.82, Ttl 4.7 (88th percentile in department)
- Fall 2007. Q1 4.5, Q3 4.7, Q4 4.6, Ttl 4.6 (88th percentile in department)
- Fall 2008. Q1 4.7, Q3 4.8, Q4 4.9, Ttl 4.8 (96th percentile in department)
- Winter 2010. Q1 4.8, Q3 4.9, Q4 4.9, Ttl 4.9 (99th percentile in department)
- Winter 2011. Q1 4.8, Q3 4.8, Q4 4.9, Ttl 4.8
- Winter 2012. Q1 4.8, Q3 4.9, Q4 4.9, Ttl 4.9
- Winter 2014. Q1 4.8, Q3 4.9, Q4 4.9, Ttl 4.9
- Winter 2015. Q1 4.7, Q3 4.8, Q4 4.8, Ttl 4.8
- Fall 2016. Q1 4.8, Q3 4.9, Q4 4.9, Ttl 4.9
- Winter 2017. Q1 4.7, Q3 4.8, Q4 4.9, Ttl 4.8
- Winter 2018. Q1 4.7, Q3 4.9, Q4 4.9, Ttl 4.8
- Fall 2018. Q1 4.8, Q3 4.9, Q4 4.9, Ttl 4.9
- Winter 2019. Q1 4.9, Q3 4.9, Q4 4.9, Ttl 4.9
- Fall 2019. Q1 4.7, Q3 4.8, Q4 4.8, Ttl 4.75
- Winter 2020. Q1 4.8, Q3 4.8, Q4 4.8, Ttl 4.8

EE 371: Introduction to Digital Circuits and Systems
Spring 2000. Q1 4.65, Q3 4.85, Q4 4.81, Ttl 4.77 (98th percentile in department, course prior ave 3.53)
Winter 2002. Q1 4.55, Q3 4.70, Q4 4.76, Ttl 4.67 (93rd percentile in department)

EE 471: Computer Design and Organization
Spring 2001. Q1 4.81, Q3 4.93, Q4 4.93, Ttl 4.89 (99th percentile in department, course prior ave 3.68)
Spring 2002. Q1 4.0, Q3 4.0, Q4 4.1, Ttl 4.03 (52nd percentile in department)
Spring 2003. Q1 4.34, Q3 4.54, Q4 4.70, Ttl 4.53 (84th percentile in department)
Spring 2004. Q1 4.8, Q3 4.9, Q4 4.9, Ttl 4.87 (99th percentile in department)
Spring 2005. Q1 4.4, Q3 4.7, Q4 4.6, Ttl 4.57 (87th percentile in department)
Spring 2007. Q1 4.53, Q3 4.87, Q4 4.87, Ttl 4.76 (96th percentile in department)
Winter 2008. Q1 4.6, Q3 4.8, Q4 4.8, Ttl 4.73 (92nd percentile in department)
Winter 2009. Q1 4.6, Q3 4.6, Q4 4.8, Ttl 4.67 (92nd percentile in department)
Autumn 2009. Q1 4.8, Q3 4.8, Q4 4.9, Ttl 4.83 (96th percentile in department)
Autumn 2010. Q1 4.9, Q3 5.0, Q4 5.0, Ttl 4.96.
Autumn 2011. Q1 4.9, Q3 4.9, Q4 4.9, Ttl 4.9.
Autumn 2013. Q1 4.7, Q3 4.7, Q4 4.6, Ttl 4.7.
Autumn 2014. Q1 4.7, Q3 4.9, Q4 4.8, Ttl 4.8
Winter 2015. Q1 4.7, Q3 4.7, Q4 4.8, Ttl 4.7
Autumn 2015. Q1 4.6, Q3 4.8, Q4 4.8, Ttl 4.7
Winter 2016. Q1 4.7, Q3 4.9, Q4 4.8, Ttl 4.8

EE/CSE 469: Computer Design and Organization
Fall 2016. Q1 4.7, Q3 4.8, Q4 4.7, Ttl 4.7
Fall 2017. Q1 4.8, Q3 4.9, Q4 4.9, Ttl 4.9
Fall 2018. Q1 4.8, Q3 4.9, Q4 4.9, Ttl 4.9
Fall 2019. Q1 4.9, Q3 4.9 Q4 4.9, Ttal 4.9

EE 541: Automated Layout of Integrated Systems
Winter 2000. Q1 4.06, Q3 4.67, Q4 4.67, Ttl 4.47 (86th percentile in department, first recent offering)
Winter 2001. Q1 4.58, Q3 4.89, Q4 4.89, Ttl 4.78 (98th percentile in department)
Winter 2002. Q1 4.65, Q3 4.84, Q4 4.81, Ttl 4.77 (97th percentile in department)
Winter 2003. Q1 4.53, Q3 4.78, Q4 4.72, Ttl 4.68 (93rd percentile in department)
Winter 2004. Q1 4.8, Q3 4.9, Q4 4.9, Ttl 4.87 (99th percentile in department)
Winter 2005. Q1 4.3, Q3 4.4, Q4 4.7, Ttl 4.47 (83rd percentile in department)
Winter 2007. Q1 4.3, Q3 5.0, Q4 4.9, Ttl 4.7 (92nd percentile in department)
Winter 2008. Q1 4.4, Q3 4.8, Q4 4.6, Ttl 4.6 (87th percentile in department)
Fall 2008. Q1 4.3, Q3 4.8, Q4 4.6, Ttl 4.6 (87th percentile in department)
Fall 2009. Q1 4.9, Q3 4.9, Q4 4.9, Ttl 4.9 (99th percentile in department)
Fall 2010. Q1 4.6, Q3 4.9, Q4 4.9, Ttl 4.8.
Fall 2011. Q1 4.9, Q3 4.9, Q4 4.9, Ttl 4.9.
Fall 2015. Q1 4.9, Q3 5.0, Q4 5.0, Ttl 5.0
Fall 2017. Q1 4.7, Q3 4.9, Q4 4.9, Ttl 4.8

Northwestern (Course prior average is the average instructor ranking for the previous 2-3 years for that course)

B01: Introduction to Digital Logic Design
Winter 1997. CTEC 5.0/6.0 (62nd percentile in department, course prior average 36th percentile)
Fall 1997. CTEC 5.6/6.0 (95th percentile in department)
Fall 1998. CTEC 5.5/6.0 (90th percentile in department)

C11: Data Structures and Data Management
Winter 1996. CTEC 3.4/4.0 (70th percentile in department, course prior average 39th percentile)

C55: Computer Architecture I
Fall 1996. CTEC 5.6/6.0 (95th percentile in department, course prior average 57th percentile)

C91: VLSI Systems Design
Spring 1996. CTEC 3.8/4.0 (97th percentile in department, course prior average 70th percentile)
Spring 1997. CTEC 5.6/6.0 (95th percentile in department)

Winter 1998. CTEC 5.4/6.0 (86th percentile in department)
Winter 1999. CTEC 5.1/6.0 (66th percentile in department)

C92: VLSI Systems Design Projects
Spring 1998. CTEC 5.0/6.0 (62nd percentile in department, first offering of course)
Spring 1999. CTEC 5.5/6.0 (90th percentile in department)

Northwestern Advisor Rating: 1996-1997 4.0/4.0 (Department average 3.2/4.0)

Student Supervision

Graduate Students Supervised

Morgan Enos, M.S., "Replication for Logic Partitioning", September 1996.

Oliver Stone, M.S., "A Comparison of ASIC Implementation Alternatives", October 1996.

Matt Hosler, M.S., "High-Performance Carry Chains for FPGAs", October 1997.

Guangyu Gu, M.S., "Accelerating Photoshop Applications with Reconfigurable Hardware", May 1999.

Venkatesh Karnam, M.S., "Applications of Reconfigurable Logic", March 2000.

Thomas Fry, M.S., "Hyperspectral Image Compression on Reconfigurable Platforms", June 2001.

Melany Richmond, M.S., "A Lemple-Ziv based Configuration Management Architecture for Reconfigurable Computing", July 2001.

Chandra Mulpuri, M.S., "Runtime and Quality Tradeoffs in FPGA Placement and Routing", July 2001.

Zhiyuan Li, Ph.D., "Configuration Management for Reconfigurable Systems", November 2001.

Katherine Compton, M.S., "Programming Architectures for Run-Time Reconfigurable Systems", Fall 1999. Ph.D. "Architecture Generation of Customized Reconfigurable Hardware", September 2003.

Todd Owen, M.S. "FPGA Implementation of Error Correction and Improved SPIHT Compression for NASA Hyperspectral Images", June 2003.

Kimberly Motonaga, M.S. "Encryption RaPiD: A Comparison of Custom and Standard-Cell Designs", December 2003.

Mark Chang, M.S., "Adaptive Computing in NASA Multi-Spectral Image Processing", Fall 1999. Ph.D. "Variable-Precision Analysis for FPGA Synthesis", July 2004.

Shawn Phillips, M.S., "Layout Generation for Application-Specific FPGAs", July 2001. Ph.D. "Automatic Layout of Customized Reconfigurable Hardware", October 2004.

Brigette Huang, M.S. "Generation of Domain-Specific 2D FPGA Architectures", Winter 2004.

Akshay Sharma, M.S., "Mapping Algorithms for Application-Specific FPGAs", December 2001. Ph.D. "Place and Route Techniques for FPGA Architecture Advancement", Spring 2005.

Mark Holland, M.S. "FPGAs in Computer Architecture Education" May 2002. Ph.D. "Automatic Creation of Product-Term Based Reconfigurable Architectures for System-on-a-Chip", Summer 2005.

Michael Beauchamp, M.S. "FPGA Architectural Support for Floating Point Computations", Summer 2006.

Peter Grossman, M.S. "Benchmarking Independence on the Triptych Architecture", Fall 2006.

Don DeWitt, M.S. "An FPGA Implementation of Statistical Based Positioning for Positron Emission Tomography", June 2008.

Ken Eguro, M.S. “Encryption-Specific FPGA Architectures”, Fall 2002. Ph.D. “Supporting High-Performance Pipelined Computation in Commodity-Style FPGAs”, November 2008.

Allan Carroll, M.S. “Characterizing the Quality of QuickRoute, A Heuristic Pipeline Router”, Fall 2008.

Nikhil Subramanian, M.S. “A C-to-FPGA Solution for Accelerating Tomographic Reconstruction”, Spring 2009.

Nathan Johnson-Williams, M.S. “Design of a Real Time FPGA-based Three Dimensional Positioning Algorithm”, Fall 2009.

Ziyuan Zhang, M.S. Winter 2010.

Ben Ylvisaker, Ph.D. ““C-Level” Programming of Parallel Coprocessor Accelerators”, Autumn 2010.

Brian Van Essen, Ph.D. “Improving the Energy Efficiency of Coarse-Grained Reconfigurable Arrays”, Autumn 2010.

Adam M. Knight, M.S. “Multi-Kernel Macah Support and Applications”, Autumn 2010.

Abhishek Raja, M.S. Autumn 2010.

Jimmy Xu, M.S. “A FPGA Hardware Solution for Accelerating Tomographic Reconstruction”, Winter 2010.

Michael Haselman, M.S. “Bitwidth Analysis of Floating-Point Computations for FPGA Implementations”, Spring 2005. Ph.D. “FPGA-Based Pulse Processing for Positron Emission Tomography”, Spring 2011.

Corey Olson, M.S. “An FPGA Acceleration of Short Read Human Genome Mapping”, Spring 2011.

Maria Kim, M.S. “Accelerating Next Generation Genome Reassembly in FPGAs: Alignment Using Dynamic Programming Algorithms” Spring 2011.

Stephen Friedman, “Resource Sharing in Modulo-Scheduled Reconfigurable Architectures”, Ph.D. Summer 2011.

James Pasko, M.S. Autumn 2011.

Andrew Price, M.S. "Hephaestus: Solving the Heterogeneous, Highly Constrained Analog Placement Problem", Winter 2012.

Marshal Barrett, M.S. Winter 2013.

Shaw-Ping “Bing” Chen, “Readout Driver Firmware Development for the ATLAS Insertable B-Layer”, M.S. Spring 2014.

Jack Lavier, Spring 2015-Summer 2015, Professional Masters Program.

Joseph Mayer, “Three Generations of FPGA DAQ Development for the ATLAS Pixel Detector”, M.S. Thesis, University of Washington, Dept. of EE, 2016.

Arushi Sonkhya, M.S. Spring 2016.

Aaron Wood, “Offset Pipelining for Coarse Grain Reconfigurable Arrays”, Ph.D. Winter 2017.

Logan Adams, M.S. Spring 2017.

Lev Kurilenko, “FPGA Development of an Emulator Framework and a High Speed I/O Core for the ITk Pixel Upgrade” M.S. Spring 2018.

Umaymah Khan, M.S. Spring 2018.

Nicholas Robillard, M.S. Spring 2018.

Nathaniel McVicar, M.S. “Architecture and Compiler Support for a VLIW Execution Model on a Coarse-Grained Reconfigurable Array” Autumn 2011. Ph.D. “FPGA Accelerated Bioinformatics: Alignment, Classification, Homology and Counting” Autumn 2018.

Dustin Werran, M.S. “Development of an FPGA Emulator for the RD53A Test Chip” Winter 2019.

Douglas G. Smith, M.S. “FPGA Development of an Emulator of the RD53A Prototype Chip and its Integration with Various Readout Systems” Spring 2019.

Richa Rao, M.S. “Implementation of Long Short-Term Memory Neural Networks in High-Level Synthesis Targeting FPGAs”, Spring 2020.

Niharika Mittal, M.S. “Development of an FPGA Emulator for the RD53B Chip”, Spring 2020.

Kelvin Lin, M.S. expected Spring 2021.

Donavan Erickson, M.S. expected Spring 2021.

Chaitanya Paikara, M.S. expected Spring 2021.

Undergraduate Student Projects Supervised

John Seng, “High-Speed Placement for Logic Emulation Systems”, Spring 1996.

Emmett Tomai, “The Trichromic Board: Reconfigurable Video Processing”, Spring 1996 - Winter 1997.

Thomas Fry, “Chimaera: Design of a Reconfigurable Functional Unit”, Summer 1996 - Spring 1998.

Jeff Kao, “VLSI Implementation of the Chimaera Reconfigurable Functional Unit”, Fall 1996 - Spring 1997.

Michael Malitsky, Felix Nayman, Yan Pechenik, Mike Yamnitsky, “Design Competition, Team: Abort, Retry, Fail; Robot: Red October”, Fall 1996 - Spring 1997.

Katherine Compton, Honors Project, “Mapping Methods for the Chimaera Reconfigurable Functional Unit”, Winter 1997 - Fall 1997.

Stephen Knol, “Data Security for Web-based CAD”, Spring 1997 - Winter 1998; Honors Project, “Logic Restructuring for Logic Partitioning”, Spring 1998 – Winter 1999; "Harnessing FPGA logic for Communication Protocols", Winter 1999 – Spring 1999.

Vernell Chapman, “Web-based Distributed Computing Infrastructure”, Summer 1997 - Fall 1997.

Dennis Kiilerich, “Software Support for the Chimaera RFU”, Fall 1997.

Doug Wilson, “Applications of Reconfigurable Hardware”, Fall 1997 - Spring 1998; Honors Project, “Configuration Compression Techniques for Reconfigurable Computing”, Summer 1998 - Fall 1998.

Jason Gonzalez, Tilman Gruber, “Design Competition, Team: Autobot”, Fall 1997 - Spring 1998.

Matt Wuebbling, “Applications of the Chimaera RFU”, Spring 1998.

Jake Brick, “Image Expansion Using Reconfigurable Logic”, Fall 1998 - Winter 1999.

Shirley Chan, “Color Space Conversion Using Reconfigurable Logic”, Fall 1998 - Spring 1999.

Ken Eguro, Honors Project, “Wavelet Compression of Image Data Using Reconfigurable Logic”, Fall 1998 - Spring 1999.

Mayank Gupta, “Fast Place & Route for Xilinx FPGAs”, Fall 1998 - Winter 1999.

Rajeev Krishna, “VLSI Chip Testing: MacTester, Logic Emulator”, Fall 1998 - Spring 1999.

Paymon Farazi, "Applications of the Chimaera RFU", Winter 1999 – Spring 1999.

Nitin Jain, “Implementation of SPIHT Compression in FPGAs”, Winter 2000 - Fall 2000.

Tim Midgett, “Instruction-set design for FPGA-based Computer Architecture Education”, Fall 2000 – Winter 2001.

James Harris, “Instruction-set design for FPGA-based Computer Architecture Education”, Fall 2000 – Spring 2001.

Jason Long, “AES Encryption on Xilinx FPGAs”, Summer 2001.

Theresa Le, “AES Encryption on Xilinx FPGAs”, Summer 2001.

Ouail Albairat, “AES Encryption on Xilinx FPGAs”, Summer 2001 – Summer 2002.

Steve Detmer, “Implementation of a MIPS processor on an FPGA”, Fall 2001.

Kevin Curtiss, “DSP Algorithms on the RaPiD System”, Spring 2002.

Ben Medina, “Encryption Algorithms on the RaPiD System”, Spring 2002.

Seung Chung, “Verilog Implementation of AES Encryption Algorithms”, Spring 2002 – Fall 2002.

Angus MacDuffie, “Image Processing Algorithms on the RaPiD System”, Summer 2001 - Spring 2003.

Michael Beauchamp, “Encryption Algorithms on the RaPiD System”, Spring 2002 – Spring 2003.

Michael Haselman, “Encryption Algorithms on the RaPiD System”, Spring 2002 – Spring 2003.

Alexander Pasciak, “Verilog Implementation of AES Encryption Algorithms”, Spring 2002 – Spring 2003.

Bruce Lam, “Layout of the Encryption RaPiD Chip”, Fall 2002 – Spring 2003.

Stephen Freeman, “FPGA Applications for LLNL”, Fall 2002 – Spring 2003.

Jason G. Louie, “Encryption Algorithms on the RaPiD System”, Winter 2003 – Spring 2003.

Daniel Hartono, “Layout of the Encryption RaPiD Chip”, Winter 2003 – Spring 2003.

Benjamin Byer, “Layout of the Encryption RaPiD Chip”, Winter 2003 – Spring 2003.

Allen Berg, “DSP Algorithms on the RaPiD System”, Spring 2002 – Summer 2003.

Gwyneth Hoi Shan Chan, “Encryption Algorithms on the RaPiD System”, Winter 2003 – Summer 2003.

Clara Lo, “Layout of the Encryption RaPiD Chip”, Winter 2003 – Summer 2003.

Nick Sherman, “Layout of the Encryption RaPiD Chip”, Winter 2003 – Summer 2003.

Jung E. Kim, “Verilog Implementations of European & Japanese Encryption Algorithms”, Spring 2003 – Summer 2003.

Daniel Scott Hippe, “Verilog Implementations of European & Japanese Encryption Algorithms”, Spring 2003 – Summer 2003.

Eka Purnama Tjung, “Verilog Implementations of European & Japanese Encryption Algorithms”, Spring 2003 – Summer 2003.

David Harold Dailey, “Verilog Implementations of European & Japanese Encryption Algorithms”, Spring 2003 – Summer 2003.

Henry Lee, “Verilog Implementations of European & Japanese Encryption Algorithms”, Spring 2003 - Summer 2003. “FPGA Support for Floating-Point Computations”, Fall 2003 – Spring 2004.

Aaron Wood, “FPGA Support for Floating-Point Computations”, Fall 2003 – Spring 2004, Fall 2004; College Honors Thesis, “The Implications of Floating Point Computations on FPGAs”, Winter 2005 – Spring 2005.

Patrick McMurchie, “Enhancements to the Independence Placer”, Fall 2004 – Winter 2005.

Jenny Bui, “Simulated Annealing Placement for the Triptych FPGA”, Winter 2005 – Spring 2005.

Jason Wong, “Retargetting Independence to the Triptych FPGA”, Winter 2005 – Spring 2005.

Courtney Wands, “VLSI Demonstrations for Educational Outreach”, Winter 2007 – Spring 2007.

Christine Steele, “VLSI Demonstrations for Educational Outreach”, Winter 2007 - Spring 2007.

Kristofer Plunkett, “Macah Implementations of K-Means Clustering”, Spring 2007.

Brian Mayton, “Macah Implementations of PCA”, Spring 2007.

Elliott Conant, “Macah Implementations of FFTs”, Spring 2007 – Summer 2007.

Nick Hunt, “Macah Implementations of FFTs”, Autumn 2007.

Jon Andes, “Macah Implementations of Signal Processing Algorithms”, Autumn 2007.

Ben Weintraub, Honors Project, “Accelerating bioinformatics algorithms on micro-parallel architectures”, Spring 2007 – Spring 2008.

Jimmy Xu, VLSI Demonstrations for Educational Outreach”, Autumn 2007 – Spring 2008.

Yuhong Wang, “Macah Implementations of Signal Processing Algorithms”, Spring 2008.

Danny Anderson, Honors Project, “Macah Implementations of Signal Processing Algorithms”, Spring 2008.

Jordan Hoyt, “Macah Implementations of PCA”, Spring 2007 – Spring 2008, Autumn 2008.

Robert Horrox, “VLSI Demonstrations for Educational Outreach”, Autumn 2007 – Winter 2008. “High-performance Computing on the Ambric Platform”, Autumn 2008. “Macah Implementations of Signal Processing Algorithms”, Winter 2009.

Chad Jerde, “Ambric Implementations of a PET Scanner”, Spring 2008, Autumn 2008 – Spring 2009.

Maria Kim, “Ambric Implementations of a PET Scanner”, Spring 2008, Autumn 2008 – Winter 2009.

Milad Hashemi, “Ambric Implementations of High-Performance Filtering”, Autumn 2008. “Macah Implementations of Signal Processing Algorithms”, Winter 2009 – Spring 2009.

Guy Bordelon, “Macah Applications Development”, Winter 2009.

Andy Turner, “Macah Applications Development”, Winter 2009 – Spring 2009.

Richard Crouch, “Macah 2.0 Application Development”, Autumn 2009 – Winter 2010.

Randy Cork, “Macah 2.0 Application Development”, Autumn 2009 – Winter 2010.

Lavanya Jandhyala, “Macah 2.0 Application Development”, Autumn 2009 – Spring 2010.

Chris Mandic, “Macah 2.0 Application Development”, Winter 2010 – Spring 2010.

Boris Kogon, “High-Speed DNA Resequencing on FPGAs”, Summer 2010 – Winter 2011.

Cooper Clauson, “High-Speed DNA Resequencing on FPGAs”, Summer 2010 – Autumn 2010.

Greg Brandt, “Applications of Macah 2.0”, Autumn 2010.

Wenbin Xu, “Applications of Macah 2.0”, Autumn 2010.

Chelsea Olson, “Applications of Macah 2.0”, Autumn 2010.

David Hough, “Shortread Resequencing in Macah 2.0”, Autumn 2010 – Winter 2011.

Tatsuro Oya, “Statistics Based Positioning in PET scanners via Macah 2.0”, Autumn 2010 – Winter 2011.

Chris Marquardt, “Wavelett filtering in Macah 2.0”, Autumn 2010 – Summer 2011.

Aravind Vadrevu, “Applications of Macah 2.0”, Winter 2011 – Summer 2011.

Bryce Kellogg, “Applications of Macah 2.0”, Winter 2011 – Summer 2011.

Serah Petersen, “High-performance Genome Resequencing”, Autumn 2011 – Spring 2012.

Hunlan Lin, “High-performance Genome Resequencing”, Autumn 2011 – Spring 2012.

Chris Gelon, “Software Support for High-Performance Genome Resequencing”, Autumn 2011 – Spring 2012.

Cody Schroeder, “Software Support for High-Performance Genome Resequencing”, Autumn 2011 – Spring 2012.

Sean Cowan, “Shortread Hardware Optimization”, Autumn 2012 – Spring 2013.

Shane Colburn, “Development of FPGA Support for the Large Hadron Collider”, Spring 2014 – Spring 2015.

Yanbo Zou, “Development of FPGA Support for the Large Hadron Collider”, Spring 2014 – Spring 2015.

Max Golub, “FPGA Support for the Large Hadron Collider”, Autumn 2014 – Spring 2016.

Bo Wang, “Development of FPGA Support for the Large Hadron Collider”, Autumn 2014 – Winter 2015.

Huaye Li, “Development of FPGA-based I/O for Educational Projects”, Winter 2015.

Kyle Gagner, “Development of FPGA-based I/O for Educational Projects”, Winter 2015 – Autumn 2015.

Jesse Liston, “Development of FPGA-based I/O for Educational Projects”, Spring 2015 – Autumn 2015.

Emmett Lam, “Caching Simulator for Computer Architecture Classes”, Spring 2015.

Vik Pandher, “Caching Simulator for Computer Architecture Classes”, Spring 2015.

Zhikun Liu, “FPGA Support for the Large Hadron Collider”, Summer 2015 – Spring 2016.

Huibo Zhao, “FPGA Support for the Large Hadron Collider”, Autumn 2015 – Winter 2016.

Weston Fiala, “FPGA Support for the Large Hadron Collider”, Autumn 2015 – Spring 2016.

Chih-Ching “Rick” Lin, “Bloom Filters on Micron’s HMC”, Spring 2016 – Autumn 2016.

Matthew McKee, “Prototyping of Verilog-based Educational Technologies”, Summer 2016.

Douglas G. Smith, “FPGA Support for the Large Hadron Collider”, Autumn 2016 – Spring 2017.

Yangming Ke, “FPGA Support for the Large Hadron Collider”, Winter 2017 - Winter 2018.

Keegan Griffee, “Using Amazon FPGA Instances for Machine Learning”, Autumn 2017 - Winter 2018.

Michael Walsh, “FPGA Support for the Large Hadron Collider”, Autumn 2017 - Spring 2018.

Ryan Linden, “Spatial Audio Processing in the SoundScape System”, Winter 2018.

Austin Oursland, “Object Recognition and Tracking in the SoundScape System”, Winter 2018.

Jerrold Erickson, “Wired Network Snooping in the SoundScape System”, Winter 2018 - Spring 2018.

Kelvin Lin, “Object Recognition and Tracking in the SoundScape System”, Winter 2018 - Spring 2018.

Tiffany Luu, “Spatial Audio Processing in the SoundScape System”, Winter 2018 – Spring 2018.

Daniel Predmore, “Wired Network Snooping in the SoundScape System”, Winter 2018 – Spring 2018.

Fred Davis, “Spatial Audio Processing in the SoundScape System”, Spring 2018.

Lirui Wang, “Spatial Audio Processing in the SoundScape System”, Spring 2018.

Sam Waddell, “Video Support on the DE-1 SoC Board”, Spring 2018.

Taylor Hartley, “FPGA Support for the Large Hadron Collider”, Spring - Autumn 2018.

Yingge “Freddie” He, “Object Recognition and Tracking in the SoundScape System”, Spring 2018 – Autumn 2018.

Maggie Fagan, “Spatial Audio Processing in the SoundScape System”, Autumn 2018 – Winter 2019

Zackery Calipse, “Spatial Audio Processing in the SoundScape System”, Autumn 2018 – Winter 2019

Yiren “Ethan” Wang, “Spatial Audio Processing in the SoundScape System”, Autumn 2018 – Winter 2019.

Cai Biesinger, “Output Video Arrays for the DE-1 SoC”, Spring 2019.

Alyssa Weed, “Output Video Arrays for the DE-1 SoC”, Spring 2019.

Jessica Lan, “FPGA Support for the Large Hadron Collider”, Spring 2018 – Autumn 2019.

Donavan Erickson, “HLS4ML: FPGA Implementation of DNNs for the Large Hadron Collider”, Winter 2019 – Spring 2019.

Kylie Lim, “HLS4ML: FPGA Implementation of DNNs for the Large Hadron Collider”, Winter 2019 – Spring 2019.

Tony Faubert, “FPGA Support for the Large Hadron Collider”, Spring 2018 – Spring 2020.

Matther Trahms, “HLS4ML: FPGA Implementation of DNNs for the Large Hadron Collider”, Winter 2019 – Spring 2020.

Lauren Choquer, “FPGA Support for the Large Hadron Collider”, Winter 2020 – Spring 2020.

Anatoliy Martynyuk, “FPGA Support for the Large Hadron Collider”, Winter 2020 – Spring 2020.

Amelia K. Dumovic, “FPGA Support for the Large Hadron Collider”, Spring 2020.

Last modified: 9/1/20