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//  Verilog for one direction of a traffic light controller

module nstoplite (clock, reset, green, yellow,red, walk, blink, dont);
input clock, reset;
output green,yellow,red, walk, blink, dont;

reg red,yellow, walk;
wire green, dont;
reg [2:0] count;

assign green = !(yellow || red);
assign dont = red || yellow;
assign blink = !(walk || red || yellow);
  always @(count) begin
    red = 1;
    yellow = 0;
    walk = 0;
    case (count)
       4, 5: begin
          red = 0;
          walk = 1;
          end
       6: red = 0;
       7: begin
          red = 0;
          yellow =1;
          end
    endcase
  end

   always @ (posedge clock) begin
      if (reset)
        begin
        count = 0;
        end
      else
        count = count + 1;
   end
endmodule
```