Chapter 6. Conclusions

In this study we wanted to generate a comparison of different fabrication technologies. A designer has many options for fabrication once a circuit has been created, and the correct choice is not always obvious. We are hoping to ease this decision by presenting the relative merits of each technology. Two of the most significant differences among the technologies are an implementation's performance and size. To quantify these, we installed and learned three CAD tools, each of which supported one of the technologies. We designed six circuits to be processed by these tools in order to achieve implementations in each of the technologies. We created full custom implementations of these six circuits as well, where each transistor was carefully placed by hand to minimize the total circuit area. Ten additional circuits were also rendered into standard cell, sea-of-gates, and FPGA implementations. Once the implementations were created, we performed a timing analysis or simulation to determine the longest path and its corresponding delay.

The data we received from the implementations gave the size of the design. Full customs designs used a third of the space needed for standard cell design. Standard cells designs were a third the size of sea-of-gates designs, and sea-of-gates designs were 19.38 times smaller than FPGA designs. The size ratio of full custom to standard cell to sea-of-gates to FPGA was thus 1:3:9:175.

Performance data was more difficult to obtain. The first step of this process was normalization so implementations at different feature sizes could be compared. We did this by analyzing the full custom MOSIS designs with four different feature sizes using Spice. The results here were odd because the delays at 1.2μ were nearly identical to the delays at 1.6μ The most likely reason for this is that the parameters for transistor models for the different feature sizes came from different sources. So many factors affect performance that using different parameters for the transistors could lead to inconsistencies.

Our next step in performance analysis was to determining the critical delay of each circuit in each technology. This also resulted in data that could not be compared because differences in the tools led to different delay estimations for the same paths. Therefore, because of inconsistancies in measuring the delays, we were unable to present a meaningful comparison of the performance of implementations in different technologies.

Another significant factor in choosing a fabrication technology is the cost involved. We gathered general pricing information which led to the conclusion that FPGA designs were cheapest until quantities reached 150. When producing between 150 and 10,000 units, gate arrays are the cheapest ASIC. Producing over 10,000 ICs is cheapest when using standard cell or full custom designs.

Apart from the issues presented here, sometimes a fabrication technology must be chosen because it is the only one with particular features. A very large or fast circuit can only be implemented in full custom. A requirement of a fast turn-around time restricts designers to FPGAs or possibly gate arrays. Reconfigurability requires FPGAs, while a requirement for non-volatility eliminates them as a choice.

Future research to enhance this study would include a successful performance comparison among the technologies. One method for achieving this would be to translate designs from each CAD tool to the full custom tool. Once each design has a duplicate version laid out, all of the designs could be extracted to implementations with the same feature size and analyzed using a single method. The problem with this is that the other CAD tools do not necessarily support the MOSIS design rules since they are targeting a specific fabrication process. Therefore the delays may be skewed by forcing the design to comply with MOSIS. A better solution would be to find a set of tools that can all work with one simulator such as Spice. There could still be problems due to different specifications in the models at different feature sizes, but this could probably be eliminated by a careful selection of model parameters.