Chapter 1. Introduction

Once a design for an integrated circuit has been conceived, a designer has four general options for its physical implementation. In the first, full custom, a designer manually designates the position of each transistor of the design on the silicon die. In a standard cell implementation, a computer designates the transistor placement by first converting the circuit to a series of basic cells contained in a library, and then arranging the cells on the die. A gate array implementation is built from a generic template of transistors. A designer defines the connections to these transistors to produce a circuit. And finally, the creation of field programmable gate array (FPGA) implementations involves programming routing and logic onto a generically designed circuit by setting SRAM in the circuit. These are four general classifications within which there are many variations, including hybrid solutions where some parts of a chip are designed with one method, while other parts use a different method.

Each of these implementation types has its advantages and disadvantages for a circuit, including different delay times for the same structures, different amounts of logic and routing resources for the same die size, volatility, design time, turn-around time, and I/O availability. These differences are discussed for each of the four general technologies. Sixteen circuit designs were used in this study to show that area requirements for an implementation increase as a design is moved from a full custom version to a standard cell version to a gate array to an FPGA. Also discussed are difficulties of comparing critical delays of circuits implemented in different technologies. A cost analysis shows how full custom and standard cell implementations become the cheapest option for large quantities of integrated circuits, while for smaller quantities gate arrays and FPGAs offer the best price per chip.

Chapter two discusses each technology in more depth, emphasizing their respective strong and weak points. Chapter three describes each circuit used in this study, and why certain circuits were included. Chapter four details the methodology used to gather our results, which are presented in Chapter five. Chapter six presents the conclusions from this study. Finally, details of the design of an efficient version of a DNA comparison circuit used in this study are presented in Appendix A, Appendix B contains the Verilog code for the circuits in this study, and Appendix C shows printouts of various implementations.