```verilog
//  Verilog for a 16-bit barrel shifter


module nbarshft (a,b,s);
input [15:0] a;
output [15:0] b;
input [3:0] s;

wire [15:0] c;
wire [15:0] d;
wire [15:0] e;

assign e = s[0] ? {a[14:0],1'b0} : a;
assign d = s[1] ? {e[13:0],2'b0} : e;
assign c = s[2] ? {d[11:0],4'b0} : d;
assign b = s[3] ? {c[7:0],8'b0} : c;

endmodule
```