Curriculum Vitae

Education

Ph.D., Computer Science & Engineering, University of Washington, 1995.
Thesis: *Multi-FPGA Systems and Rapid-Prototyping of Board-Level Designs*.
Advisors: Gaetano Borriello and Carl Ebeling.
M.S., Computer Science & Engineering, University of Washington, 1992.
B.S., Electrical Engineering & Computer Science, University of California - Berkeley, 1990.

Research Interests

Multi-FPGA Systems, FPGA Architectures and CAD tools, Rapid-Prototyping, Asynchronous Circuit and VLSI Design, Parallel Processing and Parallel Programming Languages.

Awards

AT&T Bell Laboratories Graduate Fellowship
Berkeley Honors Society
National Merit Finalist

Employment

Northwestern University, Evanston, IL
10/95 - Assistant Professor.
University of Washington, Seattle, WA
3/91- 9/95 Research Assistant. Investigated multi-FPGA systems, rapid-prototyping, asynchronous design. Developed FPGA architectures. Helped write Orca-C portable parallel programming language.
10/90 - 3/91 Teaching Assistant. Intro. to A.I. & Intro. to Operating Systems
University of California - Berkeley, Berkeley, CA
1/90 - 5/90 Reader. Graded for CS170 - Intro. to Computer Science Theory
1/87 - 5/89 Senior Engineering Aid. Participated in the design and development of the PICASSO user interface for the POSTGRES database project.
I.B.M. - T. J. Watson Research Center, Hawthorne, NY
6/89 - 12/89 Temporary Employee - Co-op. Built a framework and toolkit for a set of X11-based Common Lisp programming tools. Wrote a data object inspector, and helped write a call graph/data-flow graph inspector and debugger. System was distributed commercially by Lucid, Inc. as *XLT*.
Bell Communications Research (Bellcore), Morristown, NJ
6/88 - 8/88 Technical Summer Intern. Helped with a B-ISDN feasibility study.

Publications

Journal Articles

S. Hauck, S. Burns, G. Borriello, C. Ebeling, "An FPGA For Implementing Asynchronous Circuits", *IEEE Design & Test of Computers*, Vol. 11, No. 3, pp. 60-69, Fall, 1994.

S. Hauck, "Asynchronous Design Methodologies: An Overview", *Proceedings of the IEEE*, Vol. 83, No. 1, pp. 69-93, January, 1995.

G. Borriello, C. Ebeling, S. Hauck, S. Burns, "The Triptych FPGA Architecture", *IEEE Transactions on VLSI Systems*, December, 1995.

C. Ebeling, L. McMurchie, S. Hauck, S. Burns, "Mapping Tools for the Triptych FPGA", *IEEE Transactions on VLSI Systems*, December, 1995.

S. Hauck, G. Borriello, "An Evaluation of Bipartitioning Techniques", submitted to *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*.

Patents and Book Chapters

S. Hauck, G. Borriello, S. Burns, C. Ebeling, "Field-Programmable Gate Array for Synchronous and Asynchronous Operation", U.S. Patent 5,367,209, November 22, 1994.

J. A. Brzozowski, S. Hauck, C.-J. H. Seger, "Chapter 15: Design of Asynchronous Circuits", in J. A. Brzozowski, C.-J. H. Seger, *Asynchronous Networks*, Springer-Verlag, 1995.

Conference and Symposium Papers

S. Hauck, G. Borriello and C. Ebeling, "TRIPTYCH: An FPGA Architecture with Integrated Logic and Routing", *Advanced Research in VLSI and Parallel Systems: Proceedings of the 1992 Brown/MIT Conference*, pp. 26-43, March, 1992.

S. Hauck, G. Borriello, C. Ebeling, "Mesh Routing Topologies for Multi-FPGA Systems", *International Conference on Computer Design*, pp. 170-177, October, 1994.

S. Hauck, G. Borriello, "Logic Partition Orderings for Multi-FPGA Systems", *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, pp. 32-38, February, 1995.

S. Hauck, G. Borriello, "An Evaluation of Bipartitioning Techniques", *Chapel Hill Conference on Advanced Research in VLSI*, March, pp. 383-402, 1995.

Workshop Papers

C. Ebeling, G. Borriello, S. Hauck, D. Song, and E. A. Walkup, "Triptych: A New FPGA Architecture", *Oxford Workshop on Field-Programmable Logic and Applications*, September, 1991. Also appearing in W. Moore, W. Luk, Eds., *FPGAs*, Abingdon, England: Abingdon EE&CS Books, pp. 75-90, 1991.

E. A. Walkup, S. Hauck, G. Borriello, and C. Ebeling, "Routing-directed Placement for the Triptych FPGA", *ACM/SIGDA Workshop on Field-Programmable Gate Arrays*, February, 1992.

S. Hauck, G. Borriello, S. Burns and C. Ebeling, "Montage: An FPGA for Synchronous and Asynchronous Circuits*", 2nd International Workshop on Field-Programmable Logic and Applications*, August, 1992. Also appearing in H. Grunbacher, R. W. Hartenstein, Eds., *Field-Programmable Gate Arrays: Architectures and Tools for Rapid Prototyping*, Berlin: Springer-Verlag, pp. 44-51, 1993.

S. Hauck, G. Borriello, C. Ebeling, "Mesh Routing Topologies for FPGA Arrays", *ACM/SIGDA 2nd International Workshop on Field-Programmable Gate Arrays*, February, 1994.

S. Hauck, G. Borriello, C. Ebeling, "Springbok: A Rapid-Prototyping System for Board-Level Designs", *ACM/SIGDA 2nd International Workshop on Field-Programmable Gate Arrays*, February, 1994.

S. Hauck, G. Borriello, "Pin Assignment for Multi-FPGA Systems (Extended Abstract)", *IEEE Workshop on FPGAs for Custom Computing Machines*, pp. 11-13, April, 1994.

Technical Reports

S. Hauck, G. Borriello, “Pin Assignment for Multi-FPGA Systems”, *University of Washington, Dept. of Computer Science & Engineering Technical Report #94-04-01*, April 1994.

S. Hauck, G. Borriello, C. Ebeling, “Achieving High-Latency, Low-Bandwidth Communication: Logic Emulation Interfaces”, *University of Washington, Dept. of Computer Science & Engineering Technical Report #95-04-04*, January 1995.