Multi-Stage Amplifiers

Introduction   The objectives of this experiment are to examine the characteristics of several multi-stage amplifier configurations. Several of these will be breadboarded and measured for voltage gain, frequency response and signal swing.

In addition to the performance measurements, you should also pay attention to how the biasing of each amplifier stage is achieved, how the signal is coupled from stage to stage, and what design strategy has been adopted to desensitize the amplifier performance to variations in the transistor parameters. For each amplifier in this experiment, try to answer the question: "What has been achieved by connecting the transistors in this configuration?" To begin to answer this question, first identify whether a particular transistor is providing bias stabilization for other transistors, or is a gain stage in the signal path. Some transistors may simultaneously function in both roles. Then try to determine what components set the voltage gain of the amplifier. Track the path of the signal through the different stages of the amplifier and try to understand how much voltage gain is produced across each stage, how big the signal is at each node along the path, and what limits the signal swing at each node. Draw a schematic of the amplifier in your lab notebook and mark it up extensively to show the DC bias voltage at each node, the path that the signal takes from input to output, and any thing else that is of interest to you.

The amplifier circuits described in this experiment are not as simple as those previously used in this lab. While all of the component values are fairly close to the values needed to make the circuits work, normal variations in transistor parameters will require that each amplifier circuit be "tuned-up" slightly to center the signal swings or trim out the gain. This is left for you to do without any explicit instructions and is intended to force you to understand how the circuits work and to gain skill in electronic troubleshooting. Similarly, the procedures will only ask you to measure certain performance parameters without giving explicit instructions. At this point, you should be comfortable making all of these measurements. Refer back to experiments 2 and 3 if you need to refresh your memory on making gain and frequency response measurements.

Comment   Some of the procedures in this experiment will utilize the CA3046 npn BJT array. The CA3046 is an RCA part number, and it is the same as the National Semiconductor part number LM3046. This integrated circuit comprises five npn BJTs which are fabricated on the same piece of silicon, and is a first approximation to the behavior of BJTs that one would find in a bipolar integrated circuit. The first two BJTs are tied together with a common emitter (pin 3), and the last BJT has its emitter tied to the substrate (pin 13), as shown

in Fig. E4.0 below. All five npn BJTs have their collectors embedded into a common p-type substrate, which is connected to pin 13. In order to keep the collector-substrate pn-junctions reverse biased so that the BJTs will remain electrically isolated, the substrate on pin 13 MUST be tied to the lowest potential in the circuit, even if the fifth transistor is not being used. Any circuits using the fifth BJT of the CA3046 array MUST tie the emitter of this transistor to the lowest potential power supply rail. Failure to tie pin 13 to the lowest circuit potential will result in very unpredictable behavior for the circuit. Be warned!!
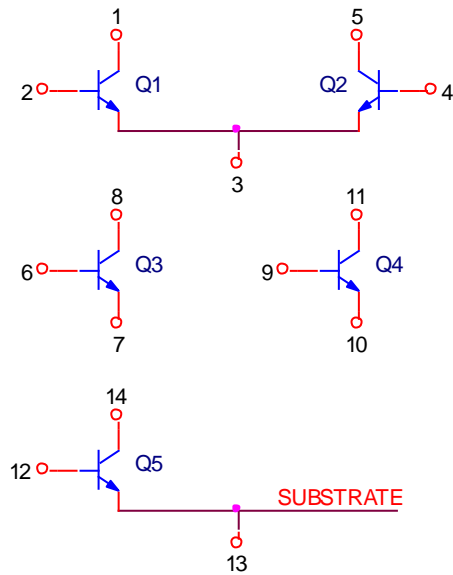

Figure E4.0

Procedure 1   Wideband CE-EF amplifier

Comment   A common-emitter (CE) stage is one of the most widely used BJT
                   configurations for obtaining both voltage and current gain. However, its gain
                   is proportional to the resistance on its collector. Attaching a heavy load (low
                   resistance) will thus reduce the gain. One simple means for improving on this
                   is to buffer the output voltage with an emitter-follower (EF) stage, also known
                   as a common-collector stage.

Set-Up   Using the solderless breadboard, construct the circuit shown in Fig. E4.1 using
                   the following components:
    R1 = 1.0 kΩ 5% 1/4 W
    R2 = 6.8 kΩ 5% 1/4 W
    R3, R5 = 3.3 kΩ 5% 1/4 W
    R4 = 100 Ω 5% 1/4 W
    C1, C2 = 10 µF electrolytic
    Q1, Q2, Q3 = CA3046 npn BJT array
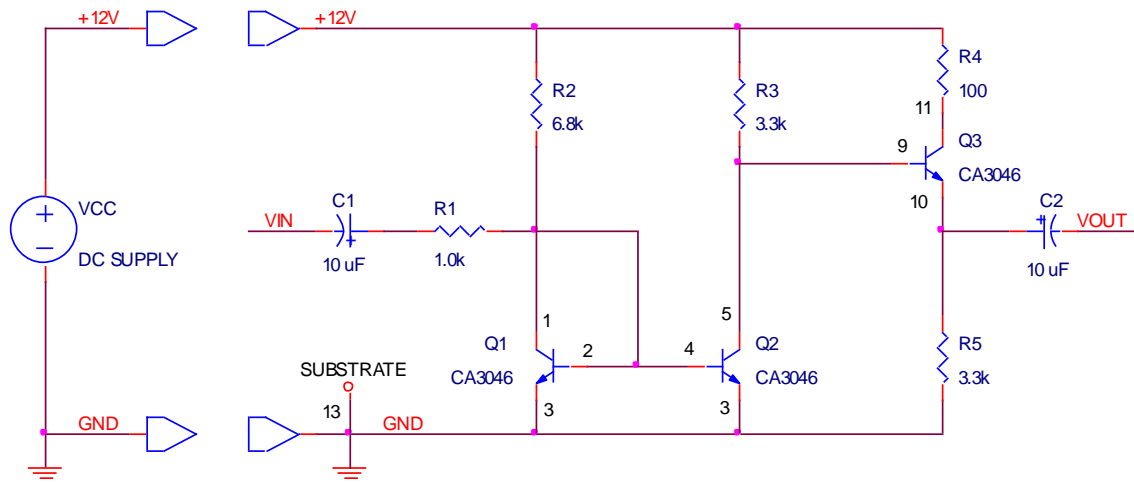

Figure E4.1

Configure a DC power supply to implement the VCC = +12.0 V DC power
supply rail, as shown in Fig. E4.1. Use a pair of squeeze-hook test leads to
connect the output of the power supply to your breadboard. Turn the DC
power supply ON and initially adjust its output to +12.0 V.

Configure a signal generator to output a 1.0 kHz sinewave with a peak-to-peak
amplitude of 1.0 Vpp. Input the signal to the free end of C1, with the signal
generator ground being connected to the ground rail of the amplifier.

Configure an oscilloscope to measure voltage versus time on both Ch-1 and
Ch-2. Start off with 5 V/div and DC coupling for both channels to probe the
signal swings and biasing. Increase the sensitivity and use AC coupling to

probe the signal amplitude. Attach both probe grounds to the ground rail of the amplifier.

Measurement-1   Adjust the circuit and signal generator to produce clean 1.0 kHz sinewaves on the input and output. Measure and record the amplitude of both input and output, and then take the ratio to determine the voltage gain.

Increase the frequency of the signal generator until the voltage gain falls to 70 percent of its value at 1.0 kHz. Measure and record this −3 dB bandwidth of the amplifier.

Restore the frequency to 1.0 kHz, and increase the amplitude of the signal generator until the output signal is clipped at both the positive and negative peaks. Measure and record the output voltage levels at which clipping occurs.

Keep this circuit set up as is. It will be only slightly modified in procedures 2 and 3.

Question-1   (a) Explain how the Q1-Q2 pair sets the bias level for Q3.
(b) Explain why the voltage gain of this amplifier is approximately given by R3/R1.
(c) Explain what sets the clipping levels for this amplifier.

Procedure 2   CE-CB cascode with EF buffer

Comment   A common-emitter (CE) followed by a common-base (CB) stage is termed a cascode. This is a very useful configuration which offers high bandwidth with good voltage and current gain.

Set-Up   Modify the circuit of Fig. E4.1 to that of Fig. E4.2 by inserting another BJT, shown as Q4, to produce the cascode. R6 will also need to be added to adjust the biasing.

R1, R6 = 1.0 kΩ 5% 1/4 W
R2 = 6.8 kΩ 5% 1/4 W
R3, R5 = 3.3 kΩ 5% 1/4 W
R4 = 100 Ω 5% 1/4 W
C1, C2 = 10 µF electrolytic
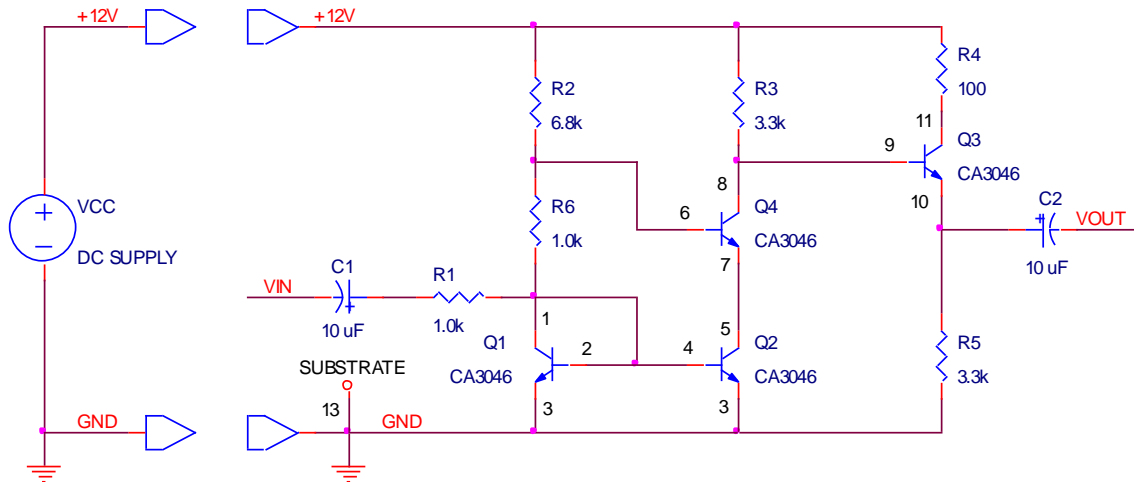Q1, Q2, Q3, Q4 = CA3046 npn BJT array

Figure E4.2

Measurement-2   Adjust the circuit and signal generator to produce clean 1.0 kHz sinewaves on the input and output. Measure and record the amplitude of both input and output, and then take the ratio to determine the voltage gain.

Increase the frequency of the signal generator until the voltage gain falls to 70 percent of its value at 1.0 kHz. Measure and record this −3 dB bandwidth of the amplifier.

Restore the frequency to 1.0 kHz, and increase the amplitude of the signal generator until the output signal is clipped at both the positive and negative peaks. Measure and record the output voltage levels at which clipping occurs.

Question-2   (a) Using your measured data, calculate the voltage gain of the amplifier in decibells (dB).

(b) Explain what determines the bias current level of Q4.

(c) Explain what advantage the addition of Q4 provides over the amplifier of procedure 1.

Procedure 3   High gain cascode

Comment   The input resistor R1 in the previous two amplifiers establishes the voltage gain and the input impedance. This stabilizes the gain against variations in transistor β, but produces a rather low value of voltage gain. By rearranging the first stage of the circuit, the input can be directly applied to the base of the input CE stage, greatly increasing its gain.

Set-Up   Modify the circuit of Fig. E4.2 to that of Fig. E4.3 by altering the connections and bias resistors around Q1 and Q2.

  R1, R6 = 100 kΩ 5% 1/4 W
  R2 = 10 kΩ 5% 1/4 W
  R3 = 4.7 kΩ 5% 1/4 W
  R4 = 100 Ω 5% 1/4 W
  R5 = 3.3 kΩ 5% 1/4 W
  C1, C2 = 10 μF electrolytic
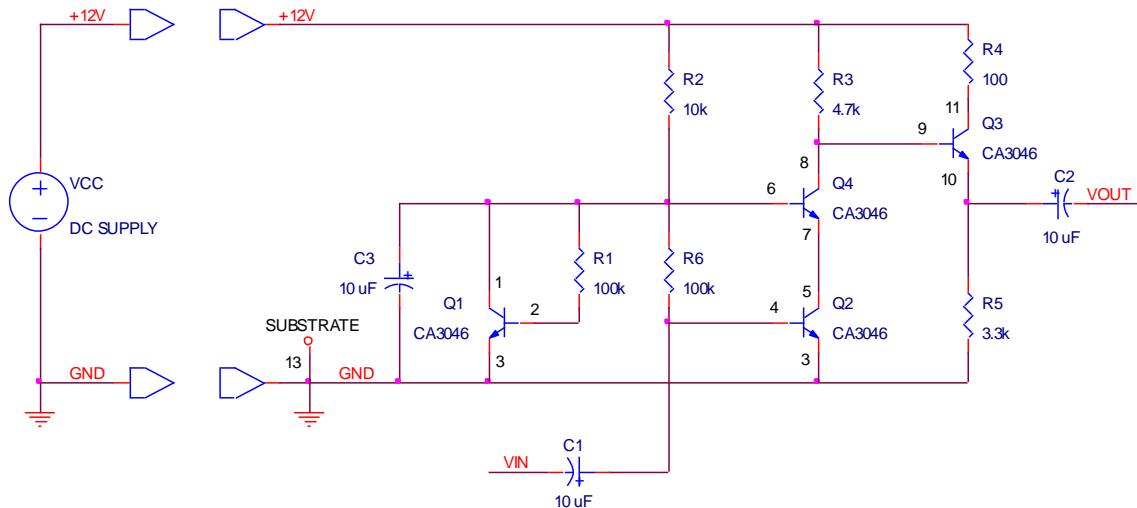 Q1, Q2, Q3, Q4 = CA3046 npn BJT array

Figure E4.3

Measurement-3   Adjust the circuit and signal generator to produce clean 1.0 kHz sinewaves on the input and output. Measure and record the amplitude of both input and output, and then take the ratio to determine the voltage gain.

Increase the frequency of the signal generator until the voltage gain falls to 70 percent of its value at 1.0 kHz. Measure and record this −3 dB bandwidth of the amplifier.

Restore the frequency to 1.0 kHz, and increase the amplitude of the signal generator until the output signal is clipped at both the positive and negative peaks. Measure and record the output voltage levels at which clipping occurs.

Question-3   (a) Using your measured data, calculate the voltage gain of the amplifier in decibells (dB).

(b) Compare the bandwidth of this amplifier to that of procedures 1 and 2 and explain the cause for the differences or similarities.

(c) Explain what function Q1 provides in this new configuration, if any.

Procedure 4   Active loads – a simple opamp

Comment
An active load usually refers to the use of a transistor's output characteristics (I_C versus V_{CE}) to provide a high output resistance but at a much larger level of DC current than what a passive resistor alone could provide. Using an active load for a common-emitter stage greatly increases the voltage gain since the collector resistance for the CE amplifier stage is now the output resistance of the active load transistor. In the circuit of Fig. E4.4, an active load is used on both collector legs of an npn differential pair. When connected like a current mirror as shown, the pair of active loads also has the benefit of routing both sides of the differential signal into the next stage, the base of Q6. The active loads in this case form a differential to single-ended converter.

Transistor Q3 provides an improved current source for the differential pair which greatly increases the common-mode rejection ratio.

Transistor Q6 implements a simple common-emitter stage with a load resistor of R8. This adds some final gain and current drive to the output pin. Resistors R5-R6-R7 provide bias stabilization for this output stage.

R4 is an optional trimpot between the emitters of Q1 and Q2. This will lower the voltage gain of this stage slightly, but it will allow the input differential amplifier to be balanced to help bias the circuit so that the output voltage will be about zero when the differential input voltage is also zero. This may or may not be necessary. If R4 is used, its value should not be more than 1.0 kΩ, or the gain of the differential amplifier will be lowered too much.

Set-Up
Construct the circuit shown in Fig. E4.4 on your solderless breadboard using the following components:
  R1 = 10 kΩ 5% 1/4 W
  R2 = 100 kΩ 5% 1/4 W
  R3 = 1.0 kΩ 5% 1/4 W
  R4 = 1.0 kΩ trimpot (if needed to balance the amplifier)
  R5 = 15 kΩ 5% 1/4 W
  R6 = 43 kΩ 5% 1/4 W
  R7 = 620 Ω 5% 1/4 W
  R8 = 3.3 kΩ 5% 1/4 W
  Q1, Q2, Q3 = 2N3904 npn BJT
  Q4, Q5, Q6 = 2N3906 pnp BJT

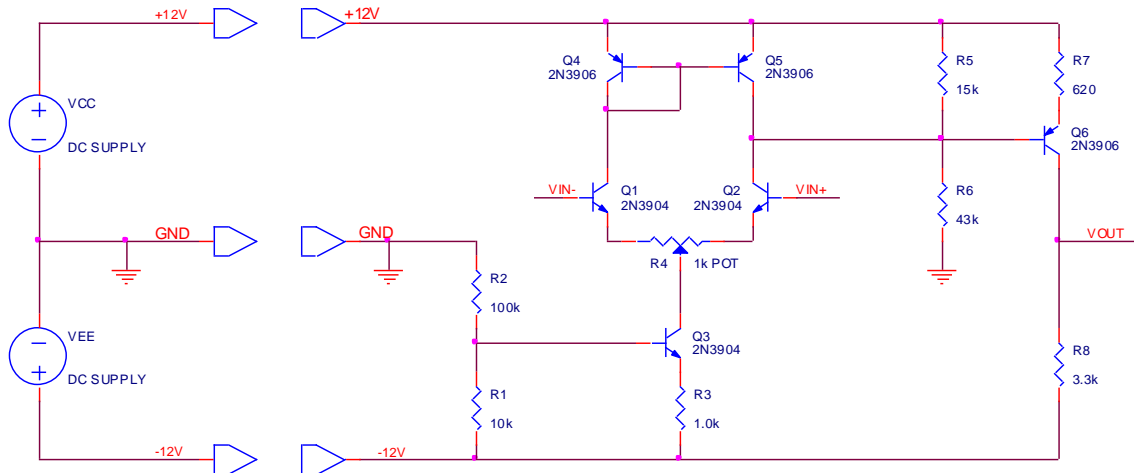Figure E4.4

Configure a dual DC power supply to implement the VCC = +12.0 V and VEE = −12.0 V DC power supply rails, as shown in Fig. E4.4. Use three squeeze-hook test leads to connect the outputs of the power supply to your breadboard. Turn the DC power supply ON and initially adjust its outputs to ±12.0 V, measured relative to the center ground terminal. This center ground terminal is the system ground.

Because of the high gain of this circuit, you may need to adjust the DC balance of the input differential amplifier. First check the balance by grounding both inputs to the bases of Q1 and Q2. Make certain that these grounds go to the system ground labeled GND in Fig. E4.4. With both inputs grounded, measure the voltage on the output pin, connected to the collector of Q6. This should be within a volt or so of ground, also. If it is not, then you may need to add in the optional trimpot R4 between the emitters of Q1 and Q2. Power down the circuit, install R4, and then fire it back up to re-measure the DC output voltage. If the output voltage is still not sufficiently close to zero, adjust the trimpot to center the output voltage to zero. You may need to readjust this balance as you go through the rest of this procedure.

Measurement-4   Ground the (−) input of the amplifier and apply a sinewave to the (+) input, relative to the system ground. Adjust the amplitude of the input to produce a non-distorted sinewave at the output. Adjust the frequency so that the maximum voltage gain is obtained. You will have to use a very small amplitude sinewave on the input, since the voltage gain of this circuit is rather high, and the frequency that you use may need to be fairly low to obtain the maximum voltage gain. Measure and record the amplitude of the input and output sinewaves, and take their ratio to determine the differential-mode voltage gain.

Increase the amplitude of the signal generator to where the output waveform is clipped at both the positive and negative peaks. Measure and record the output voltage levels at which the clipping occurs.

Decrease the amplitude of the signal generator to again produce an undistorted sinewave at the output and then increase the frequency to where the voltage gain drops to 70 percent of its maximum value. Measure and record this frequency as the -3 dB differential-mode bandwidth.

Release the (−) input from ground and apply the signal generator output to both the (+) and (−) inputs simultaneously, adjusting the amplitude to produce an undistorted sinewave at the output. Measure and record the amplitude of the input and output sinewaves and take their ratio to determine the common-mode voltage gain.

Question-4

(a) From your measured data, calculate the differential-mode voltage gain of the amplifier in decibells (dB).
(b) From your measured data, calculate the common-mode voltage gain of the amplifier in decibells (dB).
(c) Calculate the common-mode rejection ratio (CMRR) for this amplifier, expressing the result in decibells (dB).
(d) Explain what determines the clipping voltage levels.
(e) Calculate the gain-bandwidth product for this amplifier.