Experiment-3

Multi-Transistor Configurations

Introduction   The objectives of this experiment are to examine the operating characteristics of several of the most common multi-transistor configurations, including current mirrors, current sources and sinks, and differential amplifiers.

Comment   The procedures in this experiment will utilize the CA3046 npn BJT array. The CA3046 is an RCA part number, and it is the same as the National Semiconductor part number LM3046. This integrated circuit comprises five npn BJTs which are fabricated on the same piece of silicon, and is a first approximation to the behavior of BJTs that one would find in a bipolar integrated circuit. The first two BJTs are tied together with a common emitter (pin 3), and the last BJT has its emitter tied to the substrate (pin 13), as shown in Fig. E3.0 below. All five npn BJTs have their collectors embedded into a common p-type substrate, which is connected to pin 13. In order to keep the collector-substrate pn-junctions reverse biased so that the BJTs will remain electrically isolated, the substrate on pin 13 MUST be tied to the lowest potential in the circuit, even if the fifth transistor is not being used. Any circuits using the fifth BJT of the CA3046 array MUST tie the emitter of this transistor to the lowest potential power supply rail. Failure to tie pin 13 to the lowest circuit potential will result in very unpredictable behavior for the circuit. Be warned!!
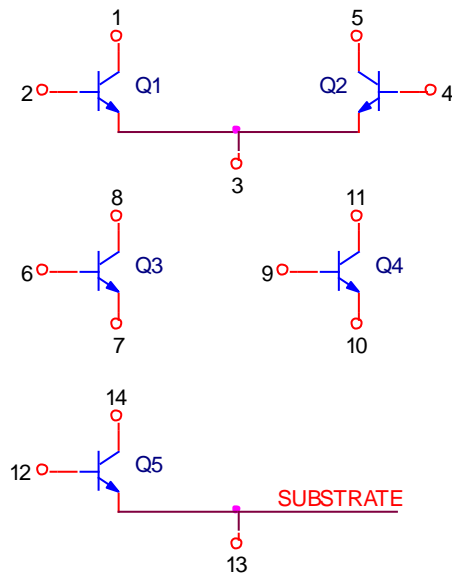

Figure E3.0

Procedure 1   Current mirror

Comment   A common need in circuit design is to establish a constant DC current for
purposes of biasing a transistor, injecting a current offset, or driving a load at a
constant value of current. Constant currents are established by current
mirrors, current sinks, and current sources, all of which are often collectively
referred to as current sources. Current mirrors replicate an existing current,
current sinks pull a fixed current into a node, and current sources push a fixed
current out of a node. All of these are based upon the forward active output
characteristics of a BJT which provide a controllable current with a typically
high value of output resistance, like an ideal current source should.

The simplest description of a BJT is that the collector current is related to the
base-emitter voltage as $I_C = I_S \exp(V_{BE}/V_T)$, where I_S and V_T are constants. A
current mirror is based upon the idea of keeping the base-emitter voltages of
two BJTs identical, by connecting them in parallel, and thus the collector
currents should also be identical. A reference current is established through
one transistor, and the second transistor "mirrors" that current into an arbitrary
load attached to its collector.

Set-Up   Using the solderless breadboard, construct the circuit shown in Fig. E3.1 using
the following components:
    R1 = 100 kΩ 5% 1/4 W
    R2 = 100 kΩ potentiometer
    Q1, Q2 = CA3046 npn BJT array

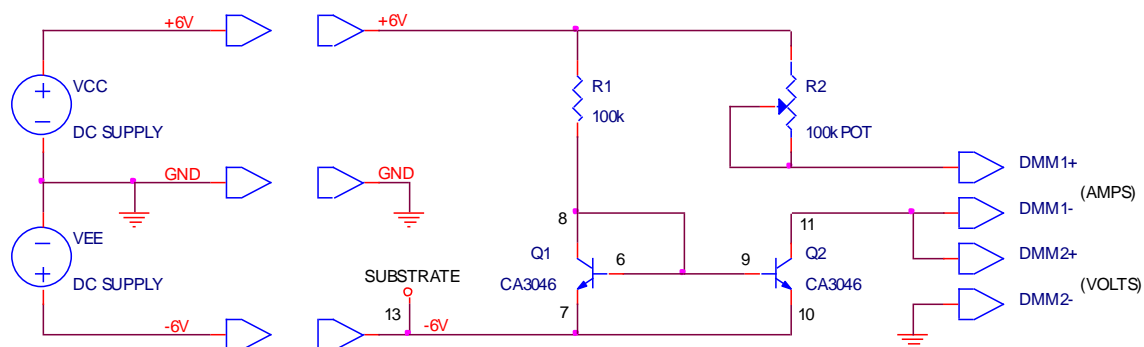Figure E3.1

Configure a dual DC power supply to implement the VCC = +6.0 V and VEE
= −6.0 V DC power supply rails, as shown in Fig. E3.1. Use a pair of
squeeze-hook test leads to connect the output of the power supply to your
breadboard. Turn the DC power supply ON and initially adjust its outputs to
±6.0 V, measured relative to the center ground terminal. This center ground
terminal is the system ground.

Connect one of the bench DMMs in series with the R2 potentiometer to measure the current flowing into the collector of Q2. Be careful to use the correct front panel banana plug jacks for this! Connect a second bench DMM to measure the voltage at the collector of Q2 relative to the system ground.

Measurement-1 Next, turn the dual DC power supply ON. Verify that the two power supply rails are at ±6.0 Volts. Adjust the R2 potentiometer to vary the collector voltage of Q2 from +6.0 V down to about −5.0 V. This simulates different load conditions. An ideal current source will keep the current constant, independent of the load conditions. To determine the ideality of this current source, take pairs of readings of the current measured on the one DMM versus the collector voltage measured on the other DMM. Suggested voltage values are +6 V, +3 V, 0.0 V, −3 V, and −5 V. Record these pairs of readings in your lab notebook. Also record the DC voltages at the base and collector of Q1.

Keep this circuit set up as is. It will be only slightly modified in procedures 2 and 3.

Question-1 (a) Calculate the output resistance of this current source as $R_{out} = \Delta V / \Delta I$, taken from your recorded data.
(b) Explain what purpose the connection between the base and collector of Q1 (pins 6 and 8) serves.
(c) Explain why the collector voltage of Q2 cannot be brought all of the way down to the lower power supply rail of VEE = −6.0 V.
(d) Explain if and how the current source is sensitive to the values of the power supply voltages.

Procedure 2   Widlar current sources

Comment
By placing a resistor in series with the emitter of one of the two transistors of a current mirror, the base-emitter voltages are no longer the same and the currents through the two transistors are scaled relative to one another. This is the principle of the Widlar current source in which the reference current can be either scaled down or scaled up. Both options will be examined in this procedure.

Set-Up
On the solderless breadboard construct the circuit of Fig. E3.2a using the following components:

R1 = 100 kΩ 5% 1/4 W
R2 = 100 kΩ potentiometer
R3 = 5% 1/4 W resistor to be calculated by you.
Q1, Q2 = CA3046 npn BJT array

This circuit can be constructed by simply starting with the circuit of procedure 1 and inserting R3 in series with the emitter of Q2.

When R3 is under the emitter of Q2 as shown, the voltage drop across R3 makes $V_{BE2} < V_{BE1}$, for which $I_{C2} < I_{C1}$. This is a reducing Widlar current source. The value of R3 to obtain a specific current from the Widlar current source is given by $R3 = [V_T \ln (I_{C1}/I_{C2})]/I_{C2}$. Calculate the value of R3 for this Widlar current source to produce $I_{C2} = 10$ μA. You should obtain a value in the range of 6-10 kΩ. Locate a standard resistor close to your calculated value and insert it into the breadboard.
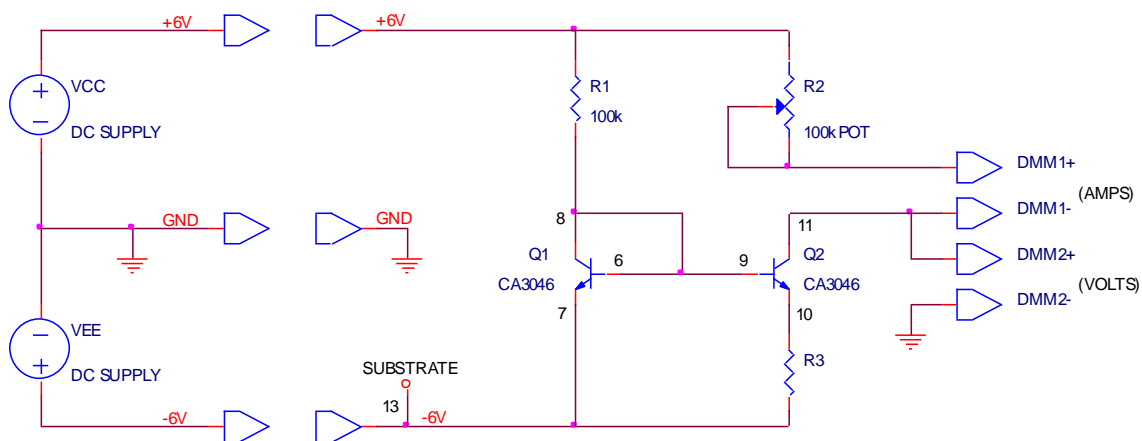

Figure E3.2a

Measurement-2a
Turn the dual DC power supply ON. Verify that the two power supply rails are at ±6.0 Volts. Adjust the R2 potentiometer to vary the collector voltage of Q2 from +6.0 V down to about +5.0 V. Because a smaller current now flows through the potentiometer R2, it will only allow the collector voltage of Q2 to be adjusted downward by about one Volt or so. Take pairs of readings of the

current measured on the one DMM versus the collector voltage measured on the other DMM and record these in your lab notebook. Also record the DC voltages at the base and collector of Q1.

More Set-up   Turn the dual DC power supply OFF, and replace R3 on the emitter of Q2 with a wire. Add a new resistor R3 in series with the emitter of Q1, as shown in Fig. E3.2b.

When R3 is under the emitter of Q1 as shown in Fig. E3.2b, the voltage drop across R3 makes $V_{BE2} > V_{BE1}$, for which $I_{C2} > I_{C1}$. This is a boosting Widlar current source. The value of R3 to obtain a specific current from the Widlar current source is given by $R3 = [V_T \ln (I_{C2}/I_{C1})]/I_{C1}$. Calculate the value of R3 for this Widlar current source to produce $I_{C2} = 1$ mA. You should obtain a value in the range of 400-500 Ω. Locate a standard resistor close to your calculated value and insert it into the breadboard.
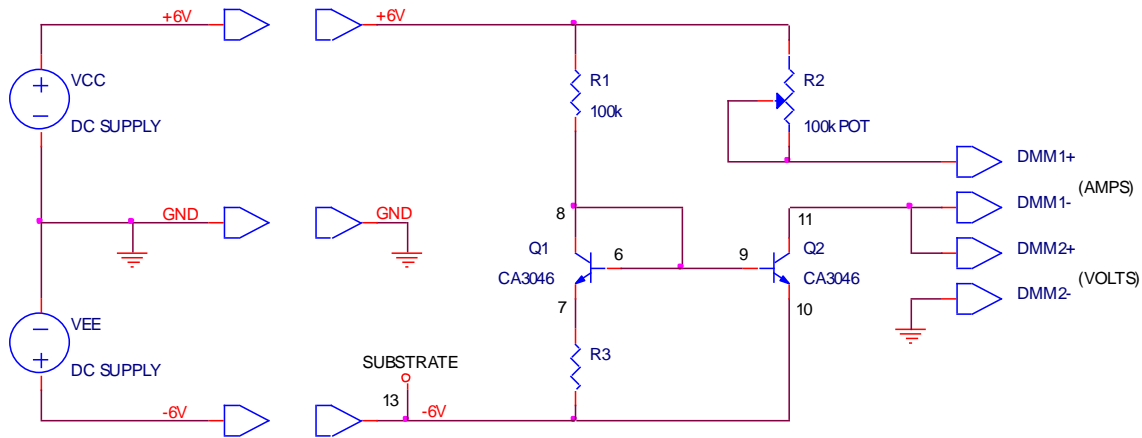

Figure E3.2b

Measurement-2b Turn the dual DC power supply ON. Verify once more that the two power supply rails are at ±6.0 Volts. Adjust the R2 potentiometer to vary the collector voltage of Q2 from +6.0 V down to about −5.0 V. Because a larger current now flows through the potentiometer R2, it can be increased to the point where Q2 saturates. Once this occurs, the output current will fall precipitously. Take readings only up to the point where Q2 saturates, probably around a collector voltage of −4.0 to −5.0 V. Take pairs of readings of the current measured on the one DMM versus the collector voltage measured on the other DMM and record these in your lab notebook. Also record the DC voltages at the base and collector of Q1.

Keep this circuit set up as is. It will be only slightly modified in procedure 3.

Question-2   (a) Calculate the output resistance of the reducing Widlar current source of Fig. E3.2a.

(b) Calculate the output resistance of the boosting Widlar current source of Fig. E3.2b.

(c) Explain why the output resistance of the reducing Widlar current source is higher than for the boosting case.

Procedure 3   Wilson current source

Comment   The output resistance of a current source is strong function of the resistance
                   which is in series with the emitter of the output transistor. One way for
                   increasing the output resistance and thus creating a more ideal current source
                   is to stack two or more transistors. The output resistance of the bottom
                   transistor is then amplified by the ones on top of it. This is the principle of the
                   Wilson current source.

Set-Up   Construct the circuit shown in Fig. E3.3 using the following components:
                       R1 = 100 kΩ 5% 1/4 W
                       R2 = 100 kΩ potentiometer
                       Q1, Q2, Q3 = CA3046 npn BJT array
                   This circuit can be constructed by simply modifying the circuit used for
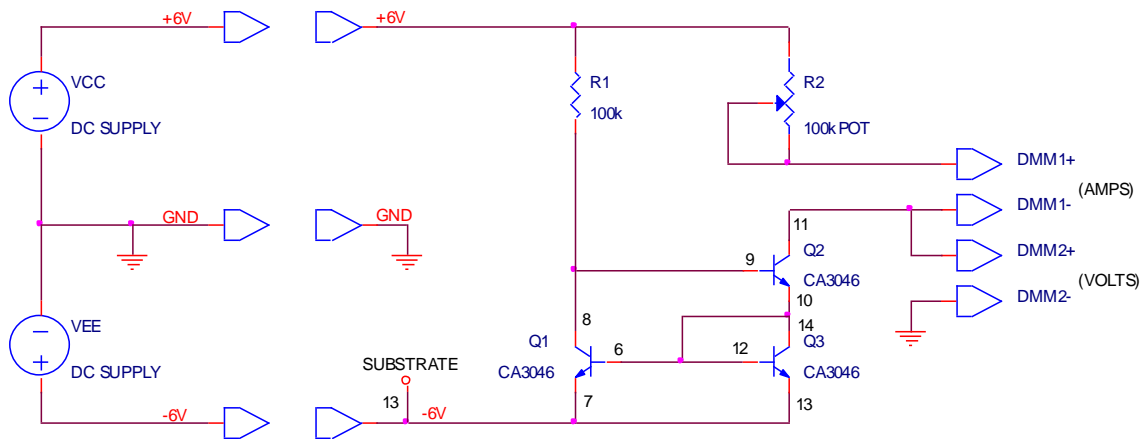   procedures 1 or 2 with the addition of the third BJT.

Figure E3.3

Measurement-3   Turn the dual DC power supply ON. Verify once more that the two power
                 supply rails are at ±6.0 Volts. Adjust the R2 potentiometer to vary the
                 collector voltage of Q2 from +6.0 V down to about −5.0 V. Take pairs of
                 readings of the current measured on the one DMM versus the collector voltage
                 measured on the other DMM and record these in your lab notebook. Also
                 record the DC voltages at the base and collector of Q1.

Question-3   (a) Using your measured data, calculate the output resistance for this Wilson
                 current source. Your data may be such that you can only say that the output
                 resistance is greater than a certain value.
                 (b) Design a current source for which the output current is exactly twice that
                 of the reference current by using three of the BJTs on the CA3046 npn array.
                 Explain in your lab notebook how this circuit achieves the factor of two
                 scaling between the reference and output currents.

Procedure 4   Emitter-coupled pair

Comment   The emitter-coupled pair is an extremely useful configuration which allows a small difference in base voltages between two BJTs to control which of the two BJTs the current flows through. This can be used for high-speed switching purposes, as in emitter-coupled logic (ECL), which will be demonstrated in this procedure. When biased just around the balance point, the emitter coupled pair forms the basis for a differential amplifier which will be examined in procedure 5.

Set-Up   Construct the circuit shown in Fig. E3.4 on your solderless breadboard using the following components:
   R1, R3 = 10 kΩ 5% 1/4 W
   R2 = 10 kΩ potentiometer
   RC1, RC2 = 330 Ω 5% 1/4 W
   RE = 1.0 kΩ 5% 1/4 W
   Q1, Q2 = CA3046 npn BJT array
   LED1, LED2 = red LEDs, identical but generic

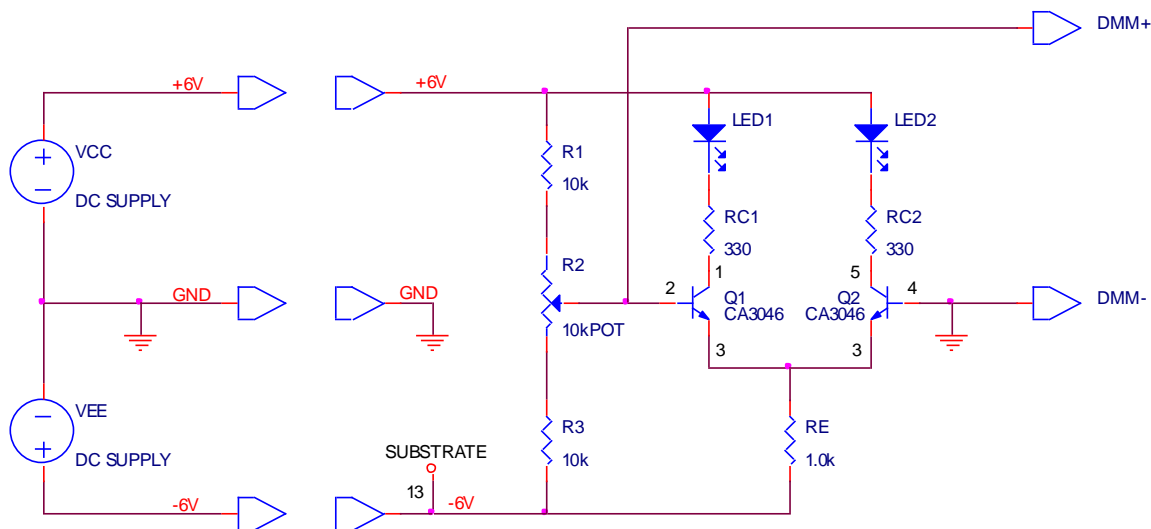
Figure E3.4

Configure a dual DC power supply to implement the VCC = +6.0 V and VEE = −6.0 V DC power supply rails, as shown in Fig. E3.4. Use a pair of squeeze-hook test leads to connect the output of the power supply to your breadboard. Turn the DC power supply ON and initially adjust its outputs to ±6.0 V, measured relative to the center ground terminal. This center ground terminal is the system ground. Connect a bench DMM to measure the voltage applied to the base of Q1 by the R1-R2-R3 voltage divider.

Measurement-4   Turn the dual DC power supply ON and verify that the rail voltages are ±6.0
V. Adjust the R2 potentiometer to set the base voltage of Q1 to exactly 0.0 V,
relative to the system ground. Both LEDs should be illuminated with equal
intensity as this is the balance point for the circuit. Adjust the R2
potentiometer until LED1 is just extinguished and record the voltage on the
base of Q1 in your lab notebook. Adjust the R2 potentiometer in the other
direction until LED2 is just extinguished and record the voltage on the base of
Q1 in your lab notebook.

Keep the circuit set up as is; it will be used again in procedure 5 after some
modifications.

Question-4   (a) What change in input voltage is required to switch the current from one
BJT to the other?
(b) Suggest a circuit modification which would allow the currents through the
two BJTs to be better equalized when the bases of the two BJTs are at
identical voltages.

Procedure 5   Differential amplifier

Comment | A differential amplifier is designed to amplify the difference between two input voltages. It is also designed to reject the average between the two input voltages. The difference between two signals is termed the differential-mode signal, while the arithmetic average of two signals is termed the common-mode signal. When only one signal is applied to, or taken from, a differential input or output, it is termed an unbalanced, single-ended or unipolar input or output. A balanced signal is a pair of signals whose magnitudes are the same but whose polarities are opposite. When a balanced signal is applied to, or taken from, a differential input or output, it is termed a balanced, double-ended, or bipolar input or output. The common-mode rejection ratio (CMRR) is the differential-mode gain divided by the common-mode gain.

Set-Up | Modify the circuit of procedure 4 to produce the circuit of Fig. E3.5 using the following components:
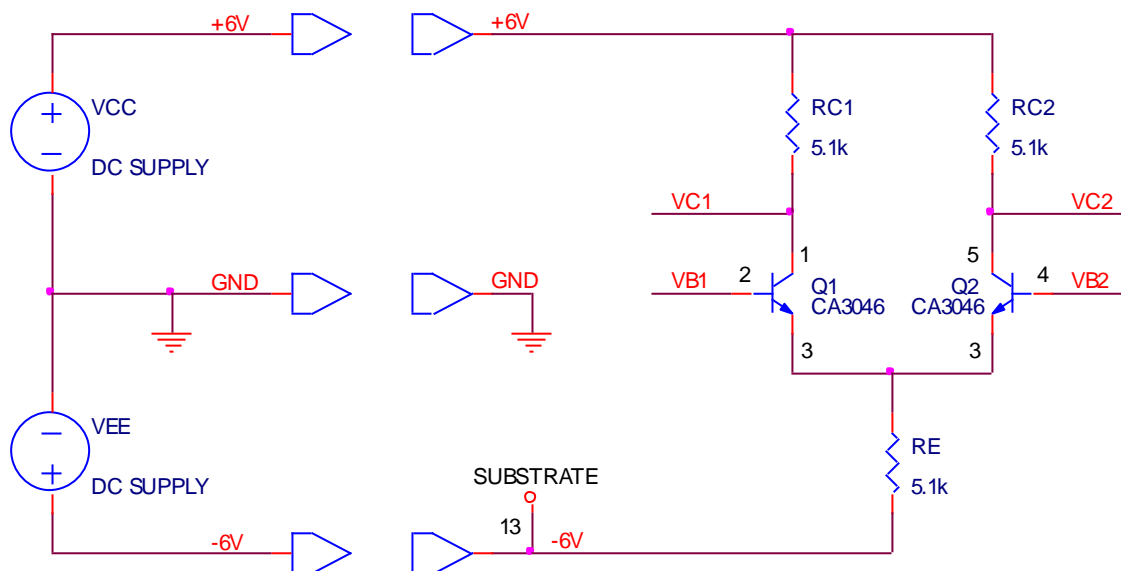RC1, RC2, RE = 5.1 kΩ 5% 1/4 W
Q1, Q2 = CA3046 npn BJT array

Figure E3.5

Ground the bases of both Q1 and Q2 by connecting them both to the system ground, i.e. the middle terminal of the dual DC power supply. Turn the dual DC power supply ON and verify that the two power rails are at ±6.0 V. Verify that both Q1 and Q2 are in the forward active region of operation by measuring the DC voltage on the emitter, base, and collector terminals of each. Voltages on the collectors of both Q1 and Q2 should be around +3 V. If this is not the case, identify and fix the problem before proceding further.

Turn the dual DC power supply OFF. Configure a signal generator to produce a 100 mVpp (peak-to-peak) sinewave at 1.0 kHz.   Make sure that any DC offset on the signal generator is turned off. Connect the ground of the signal generator to the system ground of the circuit. Disconnect the wire shorting the base of Q1 to ground. Connect the output of the signal generator to the base of Q1, node B1. The base of Q2 (node B2) remains grounded.

Connect a 10× probe to the Ch-1 and Ch-2 inputs of the oscilloscope. Configure the oscilloscope to display both channels versus time with a 1 ms/div sweep rate. Configure Ch-1 for 50 mV/div and DC coupling, and Ch-2 for 5 V/div with DC coupling. Trigger the oscilloscope off of the Ch-1 input with AC coupling of the trigger. Connect both probe ground leads to the system ground, connect the Ch-1 probe to the input of the signal generator (node B1 in Fig. E3.5), and connect the Ch-2 probe to the collector of Q1 (node C1 in Fig. E3.5).

Measurement-5   Turn the DC power supply ON to energize the circuit. You should observe about 10 cycles of the input and output sinewaves. The output sinewave, taken from the collector of Q1 should be centered about a DC level of about 3 V, and it should have an amplitude that is significantly larger than the amplitude of the input sinewave on Ch-1. Note the polarity of the output sinewave relative to the signal generator input. Move the Ch-2 probe to the collector of Q2 (node C2 in Fig. E3.5) and again note the polarity of the output sinewave relative to the signal generator input. You should observe that the amplitudes of the two signals on C1 and C2 are the same.

Adjust the amplitude of the signal generator so that the output sinewave is as large as possible, but not yet clipping on either polarity peak. Calculate the voltage gain of the amplifier by dividing the amplitude of the output sinewave by the amplitude of the input sinewave and record the result in your lab notebook. Note that this voltage gain represents that from a double-ended input to a single-ended output. This is because the input signal is applied between the bases of the two transistors, but the output is taken from only one of the collectors. (A double-ended output would have been taken from between the two collectors.) This voltage gain is the differential voltage gain of the amplifier.

Adjust the amplitude of the signal generator until the output sinewave is not clipped. Increase the frequency of the signal or function generator until the amplitude of the output sinewave has fallen to about 70 percent of its initial value at 1 kHz. This will probably occur around 1 MHz, so the oscilloscope and the input signal will need to have their time bases adjusted together to retain 5-20 complete cycles on the oscilloscope display. Record in your lab notebook the frequency at which the ratio of the output to input amplitude has

fallen to the 70 percent point. This is the –3 dB bandwidth for the differential gain of this amplifier.

Next, disconnect the wire shorting the base of Q2 to ground and connect the bases of Q1 and Q2 together and to the signal generator. This will apply a common-mode input signal to the differential amplifier from which the common-mode gain can be determined. Configure the signal generator to produce a 1.0 kHz sinewave with a peak-to-peak amplitude of 3 Vpp. Adjust both Ch-1 and Ch-2 gains on the oscilloscope to 2 V/div. Move the Ch-2 probe to and from C1 and C2, noting the polarity of the output waveforms relative to the signal generator input. Measure the common-mode gain of the differential amplifier by taking the ratio of the output amplitude at either C1 or C2 to the input amplitude at either B1 or B2 and record this in your lab notebook.

Using the procedures described previously, measure the –3 dB bandwidth of the common-mode gain and record this in your lab notebook.

Finally, configure the signal generator to produce a +5.0 V positive DC offset on its output signal, while it is still connected to produce a common-mode input signal. Measure and record the common-mode gain in your lab notebook, noting carefully the polarity of the output waveforms relative to the input signal.

Question-5   (a) Calculate the common-mode rejection ratio (CMRR), expressing it in both as a pure ratio and in decibells (dB).
(b) Explain why the common-mode gain is approximately 0.5 and inverting when no DC offset is applied from the signal generator.
(c) Explain why the common-mode gain jumps to approximately 1.0 and becomes non-inverting when a +5.0 V DC offset is applied from the signal generator. This is a tricky question! But it represents a situation which often occurs in the lab and which confuses people. Try to figure this one out – it will add greatly to your ability to troubleshoot analog circuits.
(d) Suggest a way to increase the CMRR of this differential amplifier. Hint: think about how ideal the current source RE is and how it might be improved.