Experiment-2

Single-Stage BJT Amplifiers

Introduction

The objectives of this experiment are to observe the operating characteristics of the three fundamental single-stage BJT amplifiers: common-emitter, common-base, and common-collector, and to learn how to properly bias a BJT for small-signal amplification.

Biasing a BJT into the forward-active region of operation is the first required step in creating an amplifer stage. Once the BJT is properly biased, various amplifier stages can be achieved by injecting a signal into one terminal and extracting a signal from another.

When the BJT is regarded as a two-port network, one of the terminals must serve as a common point between the input port and the output port. If the input is on the base and the output on the collector, the emitter must therefore be common between the input and output ports, and the configuration is referred to as a common-emitter (CE) amplifier stage.

Two rules apply to single stage BJT amplifiers: the base can never be an output, and the collector can never be an input. With these rules, there are three fundamental BJT amplifier stages: (1) a common-emitter (CE) where the input is on the base and the output on the collector, (2) a common-base (CB) where the input is on the emitter and the output on the collector, and (3) a common-collector (CC), also known as an emitter-follower (EF) where the input is on the base and the output is on the emitter.

This laboratory experiment will examine the characteristics of each of these three fundamental amplifer configurations.

Procedure 1 NPN common-emitter stage characteristics

Comments

With in input signal delivered to the base terminal and the output signal pulled from the collector terminal, the emitter terminal of the BJT is common to the input and output ports. Thus, this configuration is termed a common-emitter transistor stage.

In the following circuit a potentiometer R3 will be used to adjust the value of the collector resistor. To keep the value of this resistance from accidentally being reduced all the way to zero, an additional "pot-stop" resistor R2 is added in series to establish a minimum resistance for this branch. This is always good practice for potentiometers to avoid producing unwanted short circuits which could cause serious circuit problems, in this case destroying the transistor. Whenever you design a circuit with a potentiometer in it, always consider the worst cases that will occur at each of the two endpoints of the potentiometer's settings. A little forethrought can save parts and frustration later!

Set-Up

Using the solderless breadboard, construct the circuit shown in Fig. E2.1 using the following components:

R1 = 100 kΩ 5% 1/4 W
R2 = 330 Ω 5% 1/4 W
R3 = 5 kΩ potentiometer
Q1 = 2N3904 npn BJT

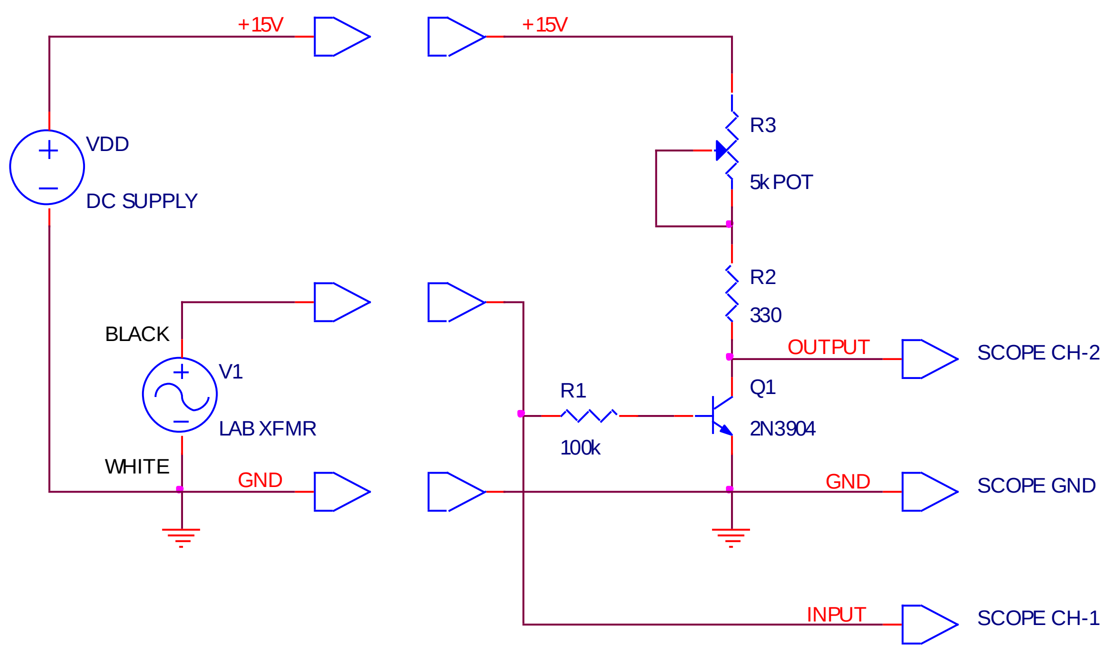

Figure E2.1

Turn the power switch OFF on the laboratory transformer and plug the unit into a 120 VAC line receptacle. Connect the transformer to the circuit board using leads from the black and white banana jacks as shown in Fig. E2.1. This will apply a 10 V peak sinewave to the circuit once the power is turned on.

Configure a DC power supply to implement the VCC DC source in Fig. E2.1. Use a pair of squeeze-hook test leads to connect the output of the power supply to your breadboard. Turn the DC power supply ON and initially adjust its output to +15.0 Volts. Initially adjust the R3 potentiometer for a value of zero ohms, i.e. the series combination of R2 + R3 should be just R2 = 330 Ω.

Connect a 10× probe to the BNC connectors on each of the two input channels of an oscilloscope. Connect the probe from Ch-1 to the input end of R1 to monitor the input signal, and connect the probe from Ch-2 to the output node between R2 and Q1 to monitor the output signal, as shown in Fig. E2.1. Both oscilloscope probe ground leads and the ground lead from the DC power supply should all be connected to the emitter lead of transistor Q1. Configure the oscilloscope to display both channels with a vertical scale of 5 V/div, which includes the attenuation of the 10× probes. Set the input coupling of both channels to DC, and make sure that channel-2 is not inverted. Set the timebase to 5 ms/div. Set the trigger mode to AUTO with a source of Ch-1. Finally center both traces on the center of the screen by switching the input coupling for each channel to GND, moving each trace to the center hairline of the screen using the position controls, and then returning the input coupling switches to the DC position.

Measurement-1 Next, turn the laboratory transformer ON. At this point, the oscilloscope should show a sinewave input for Ch-1 and only the positive half cycles of a sinewave output for Ch-2. Sketch both of these waveforms on the same set of axes in your lab notebook.

The oscilloscope will now be used to directly display the voltage transfer characteristics (VTC) of this circuit. Do not change any of the connections from those of Fig. E2.1 and simply reconfigure the oscilloscope to display Ch-1 versus Ch-2 in an X-Y mode. Ground the inputs to both channels by setting the coupling switches to GND, and then switch the oscilloscope into the X-Y mode. Use the position controls to move the dot onto the cross-hairs in the exact center of the screen. Change the input coupling on each of the two channels back to DC and the display should now show the VTC. Sketch the VTC shown on the oscilloscope screen in your notebook.

Using the built-in meter on the DC power supply, vary the output voltage VCC over the range of 0.0 to +15 Volts. Switch back and forth between the voltage versus time and VTC (X-Y) modes of the oscilloscope to observe the effect on the output waveforms and the VTC. Jot down in your notebook the effect of varying the power supply voltage.

Now examine how the VTC is affected by the value of collector resistance, R2 + R3. Vary the R3 potentiometer from 0 to 5 kΩ and switch the oscilloscope back and forth between displaying the VTC and displaying the voltage versus time waveforms to better appreciate what is happening in the circuit and how this is represented on the VTC. For larger values of R2 + R3, the VTC should have three distinct segments. Identify the region of transistor operation for each of these as: {cutoff, forward active, reverse active, or saturated}.

Question-1

(a) From the measured VTC, is the npn common emitter stage inverting or non-inverting?
(b) Explain why the VTC does not exhibit a saturation segment when the value of R2 + R3 is reduced to below a certain point.
(c) Explain why R1 is needed in the circuit of Fig. E2.1. I.e., why can't the lab transformer be directly connected to the base of Q1? If this totally stumps you, short out R1 in the circuit and see what happens; just be prepared to buy a new 2N3904 from the stockroom, along with some new transformer fuses!

Procedure 2 PNP complement to the common-emitter stage

Comment

Every transistor circuit has a complement which is constructed by reversing the power supply polarities and reversing the sex of each transistor. If the parameters for each device are maintained, the performance of the complementary circuit will be symmetrical to that of the original. It is often easier to learn the characteristics of one type of circuit, say npn, and then simply take to complement to remember how the pnp version behaves. Procedure 2 duplicates procedure 1, but with the pnp complementary circuit.

Set-Up

On the solderless breadboard construct the circuit of Fig. E2.2 using the following components:

R1 = 100 kΩ 5% 1/4 W resistor
R2 = 330 Ω 5% 1/4 W resistor
R3 = 5 kΩ potentiometer
Q1 = 2N3906 pnp BJT

This circuit can be constructed by simply replacing the Q1 transistor of procedure 1 with a type 2N3906 and reconfiguring the power supply to be negative on the collector of Q1.

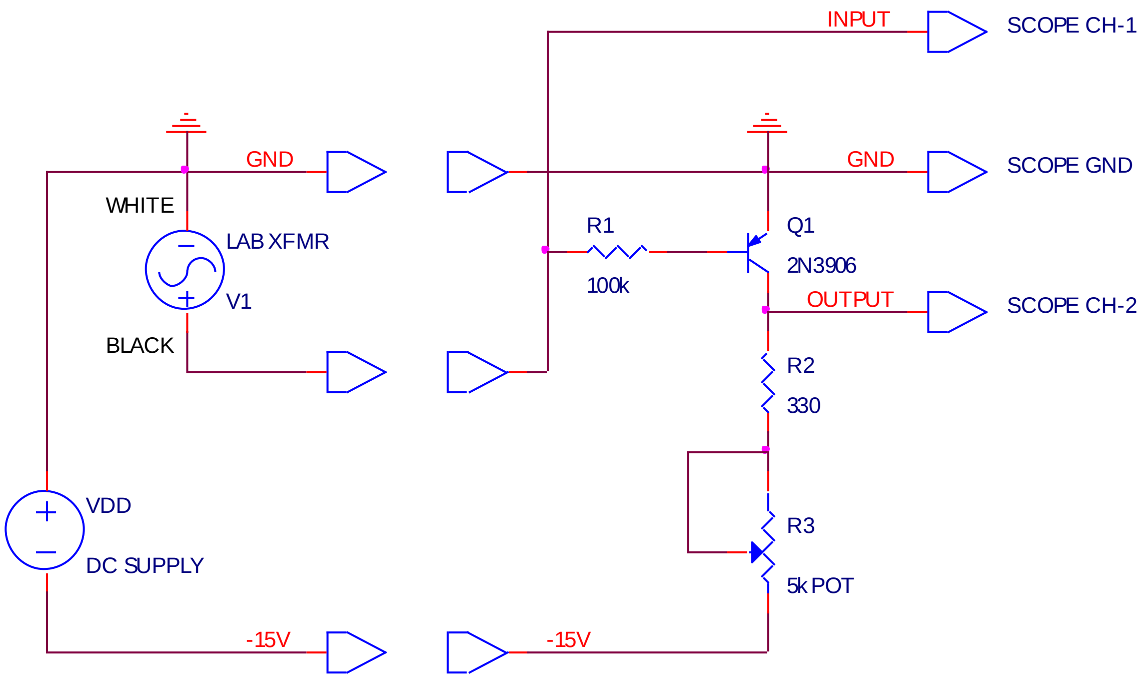

Figure E2.2

Note that both oscilloscope probe grounds are again connected to the emitter terminal of Q1, but that the more *positive* terminal of the DC power supply is connected to the emitter.

Turn the power switch OFF on the laboratory transformer and plug the unit into a 120 VAC line receptacle. Connect the transformer to the circuit board using leads from the black and white banana jacks as shown in Fig. E2.2. This will apply a 10 V peak sinewave to the circuit once the power is turned on.

Configure a DC power supply to implement the VCC DC source in Fig. E2.2. Use a pair of squeeze-hook test leads to connect the output of the power supply to your breadboard. Turn the DC power supply ON and initially adjust its output to −15.0 Volts. Initially adjust the R3 potentiometer for a value of zero ohms.

Connect a 10× probe to the BNC connectors on each of the two input channels of an oscilloscope. Connect the probe from Ch-1 to the input end of R1 to monitor the input signal, and connect the probe from Ch-2 to the output node between R2 and Q1 to monitor the output signal, as shown in Fig. E2.2. Configure the oscilloscope to display both channels with a vertical scale of 5 V/div, which includes the attenuation of the 10× probes. Set the input coupling of both channels to DC, and make sure that channel-2 is not inverted. Set the timebase to 5 ms/div. Set the trigger mode to AUTO with a source of Ch-1. Finally center both traces on the center of the screen by switching the input coupling for each channel to GND, moving each trace to the center hairline of the screen using the position controls, and then returning the input coupling switches to the DC position.

Measurement-2 Next, turn the laboratory transformer ON. At this point, the oscilloscope should show a sinewave input for Ch-1 and only the negative half cycles of a sinewave output for Ch-2. Sketch both of these waveforms on the same set of axes in your lab notebook.

The oscilloscope will now be used to directly display the voltage transfer characteristics (VTC) of this circuit. Do not change any of the connections from those of Fig. E2.2 and simply reconfigure the oscilloscope to display Ch-1 versus Ch-2 in an X-Y mode. Ground the inputs to both channels by setting the coupling switches to GND, and then switch the oscilloscope into the X-Y mode. Use the position controls to move the dot onto the cross-hairs in the exact center of the screen. Change the input coupling on each of the two channels back to DC and the display should now show the VTC. Sketch the VTC shown on the oscilloscope screen in your notebook.

Using the built-in meter on the DC power supply, vary the output voltage VCC over the range of 0.0 to −15 Volts. Switch back and forth between the voltage versus time and VTC (X-Y) modes of the oscilloscope to observe the effect on the output waveforms and the VTC. Jot down in your notebook the effect of varying the power supply voltage.

Now examine how the VTC is affected by the value of collector resistance, R2 + R3. Vary the R3 potentiometer from 0 to 5 kΩ and switch the oscilloscope back and forth between displaying the VTC and displaying the voltage versus time waveforms to better understand what is happening. For larger values of R2 + R3, the VTC should have three distinct segments. Identify the region of transistor operation for each of these as: {cutoff, forward active, reverse active, or saturated}.

Question-2

(a) From the measured VTC, is the pnp common emitter stage inverting or non-inverting?

(b) From the recorded VTCs, estimate the voltage gain of the stage when it is used as an amplifier with the transistor Q1 in the forward active region of operation. Note: the voltage gain will be the slope of the VTC.

(c) Verify that the voltage gain of the common emitter stage is proportional to the value of the collector resistance. Do this by dividing the voltage gain by RC = R2 + R3 = 330 Ω, and by RC = R2 + R3 = 5330 Ω, at the two limits of travel for the potentiometer.

Procedure 3 Biasing up an npn stage

Comment

The first step in designing or building an amplifier is getting the transistor biased into the correct region of operation, which is nearly always the forward active region. This can vary from transistor to transistor, since the β and other parameters to which the bias is sensitive may vary over quite a range for a given transistor type. Troubleshooting malfunctioning transistor amplifier circuits can almost always be accomplished by simply checking the biasing with a DMM to insure that the voltages on each terminal are in the correct voltage relationship to each other. Use this procedure to become acquainted with what a properly biased BJT "looks like" with a DMM so that you can then recognize an improperly biased one later on.

Set-Up

The resistor values are going to be chosen by you as you progress through the measurement part of this procedure!

R1, R2, RE, RC = 5% 1/4 W resistors, values to be chosen
Q1 = 2N3904 npn BJT

The circuit you will construct is shown in Fig. E2.3.

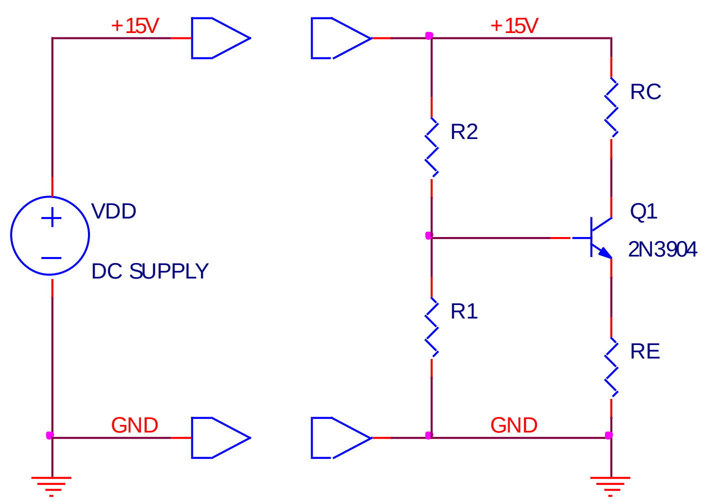

Figure E2.3

Begin by establishing +15.0 V and Gnd (ground) power supply rails on your solderless breadboard. Keep the power supply turned OFF, and only turn it ON briefly to check a voltage value while you are assembling this circuit. This is a good practice to get into the habit of doing. Always drop the power to a circuit while you are making changes to it. While plugging and unplugging parts on the breadboard, you can very easily subject the devices to over-voltage or over-current which could destroy them. Dropping the power assures that this will not occur. And take heart; you circuit will "boot-up" in a millisecond or less, far faster than Windows!

Measurement-3 The first step in biasing a transistor is establishing the base voltage. This will be done through the resistor voltage divider chain of R1 and R2. Design a voltage divider chain of R1 and R2 that puts the base voltage at approximately 1.5 V, relative to ground. Pick values for R1 and R2 that give a voltage division ratio of 10:1 (to give 1.5 V from the 15 V power rail) and which runs about 150 μA through it. The expected base current used by Q1 will be around 10 μA or less, so making the current flow through R1 and R2 about 15 times this value should make the voltage between R1 and R2 nearly independent of the level of base current. Locate these resistors, plug them into the breadboard, and briefly power up the circuit to verify that the node between R1 and R2 is at approximately 1.5 V. Record your measured voltage in your lab notebook.

With the base voltage at about 1.5 V, the emitter voltage will then be approximately 0.7 V less than this, or at about 0.8 V. Pick a value for RE so that the 0.8 V across RE produces a current flow of about 0.8 mA, which is to be the emitter current of Q1. Plug Q1 into the breadboard, connecting its base to the node between R1 and R2, and connecting its emitter to the Gnd rail through the RE that you have chosen. Leave the collector unconnected for the moment. Power up the circuit and measure the base and emitter voltages, recording the results in your lab notebook. They should measure lower than the values you designed for because Q1 is not yet acting like a transistor. With the collector open-circuited, the base-emitter junction behaves only as a diode, which turns on and puts RE and R1 almost in parallel. The heavier value of base current in this case pulls the base voltage down below your design value. Power the circuit OFF, connect the collector of Q1 to the +15 V power rail. Briefly power the circuit ON, remeasure the base and emitter voltages, and record these in your lab notebook. Since the emitter current is now being supplied by the collector connection, the base current is much lower now, and the base voltage should be closer to your design value of around 1.5 V.

Assuming that the emitter and collector currents are now both about 0.8 mA, choose a value for RC to drop the collector voltage down to about +10 V, relative to the Gnd rail. Turn the power supply OFF, insert your value of RC into the collector branch, briefly turn the power back ON and measure the emitter, base, and collector voltages of Q1, each relative to the Gnd rail. Record all three of these in your lab notebook.

At this point, you should have a properly biased-up npn BJT, ready to turn into an amplifier! Remember that transistor amplification requires that the BJT be operated in the forward active region, which is what the biasing exercise is attempting to produce. Forward active operation requires a forward-biased base-emitter junction and a reverse-biased base-collector junction. Review your measured values of emitter, base, and collector voltages and verify that this is correct for forward-biasing an npn BJT. If in the future you encounter a BJT which is not behaving properly as an amplifier, first check it to insure that it is biased up properly so that its terminal voltages have the same voltage relationships as the BJT in this procedure. The ability to rapidly troubleshoot transistor biasing problems will put you way ahead in the game of building amplifiers!

Save this circuit! It will be used in the next four procedures.

Question-3 From your measured values of V_E, V_B, and V_C, calculate the current flowing through each resistor, and the emitter, base, and collector currents for the transistor. Verify that the terminal currents for the transistor sum to zero (Kirchoff's Current Law). Calculate the value of β for the transistor in this bias state.

For a forward-active npn BJT, order the emitter, base, and collector terminals in increasing voltage. For a forward-active pnp BJT, order the emitter, base, and collector terminals in increasing voltage.

Procedure 4 Common-emitter amplifier

Comment

In the next four procedures, the biased-up npn BJT of procedure 3 will be employed as four different types of single-stage amplifiers. These next four procedures will all be similar; as you move through them, take note of the differences between the behavior of the different amplifier configurations.

Set-Up

Starting from the biased-up npn BJT of procedure 3, add two capacitors C1 and C2 as shown below in Fig. E2.4. Do not yet connect the (−) leads of the capacitors.

C1, C2 = 10 μF electrolytic capacitors

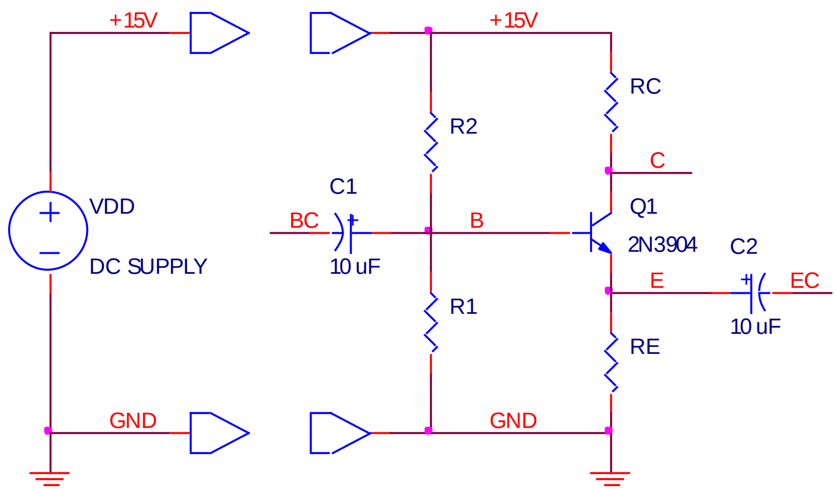

Figure E2.4

Configure a signal generator or function generator to produce a 1.0 Vpp (peak-to-peak) sinewave at 1.0 kHz. Connect the ground of the signal or function generator to the Gnd rail of the circuit. Connect the output of the signal or function generator to the (-) end of capacitor C1 (node BC in Fig. E2.4). The (-) end of capacitor C2 (node EC in Fig. E2.4) remains unconnected throughout this procedure.

Connect a 10× probe to the Ch-1 and Ch-2 inputs of the oscilloscope. Configure the oscilloscope to display both channels versus time with about 1 ms/div sweep rate. Configure both inputs to DC coupling with 5 V/div gain. Trigger the oscilloscope off of the Ch-1 input with AC coupling of the trigger. Connect both probe ground leads to the Gnd power rail, connect the Ch-1 probe to the (−) end of C1 where the signal or function generator is input (node BC in Fig. E2.4), and connect the Ch-2 probe to the collector of Q1 (node C in Fig. E2.4).

Turn the DC power supply ON to energize the circuit. You should observe about 10 cycles of the input and output sinewaves. The output sinewave, taken from the collector of Q1 should be centered about a DC level of about 10 V, and it should have an amplitude that is significantly larger than the amplitude of the input sinewave on Ch-2. If so, then congratulations on making your first amplifier! Now let's measure how well it works.

Measurement-4 Calculate the gain of this amplifier by taking the ratio of the output to input amplitudes, and record this in your lab notebook. Make sure that both the input and output sinewaves are not clipped or distorted in any way. If they are, reduce the amplitude of the input sinewave until nice clean looking sinewaves are present at both input and output terminals. Also note in your lab notebook the polarity of the output sinewave relative to the applied input signal.

Slowly increase the amplitude of the input sinewave until the output sinewave begins to clip. Note the voltage relative to the Gnd power rail at which this occurs and whether the clipping is on the positive or negative polarity peaks of the sinewave.

Keep increasing the amplitude of the input sinewave until the other polarity peak of the sinewave output begins to clip and note the voltage at which this occurs, relative to the Gnd power rail. After recording the clipping points in your lab notebook, decrease the amplitude of the signal or function generator until a pure sinewave is again obtained at the output.

A key performance parameter for the amplifier is its bandwidth, or how high in frequency it will maintain the voltage gain that it is now exhibiting at 1 kHz. As the input frequency is increased on the function or signal generator, the amplitude of the input sinewave should remain constant, but beyond a certain frequency, the amplitude of the output sinewave will start to drop. The –3 dB bandwidth of the amplifier is where the output signal amplitude has dropped by a factor of $\sqrt{2} = 1.414$, or down to roughly 70 percent of its former amplitude. To find this frequency, keep increasing the frequency of the signal or function generator until the output sinewave has fallen to about 70 percent of its present amplitude. You may need to readjust the oscilloscope sweep rate by several decades, as the –3 dB frequency should lie around 1 MHz or so. Monitor both the input and output sinewaves as you increase the frequency. While the signal generator should remain nearly constant in amplitude, there will be a point where its output will also fall with increasing frequency. The objective of this measurement is to determine the frequency response of the amplifier, not the signal generator, so you will always want to look at the ratio of the output and input amplitudes. Record in your lab notebook the –3 dB bandwidth of this common-emitter amplifier.

Keep the circuit set up as is; it will be used again in procedure 5 with only a minor modification.

Question-4

(a) Is the common-emitter amplifier inverting or non-inverting?
(b) Suggest a redesign of the amplifier to increase the upper clipping voltage.
(c) Suggest a redesign of the amplifier to decrease the lower clipping voltage.
(d) When the input is capacitor coupled through C1, what is the DC voltage gain of this amplifier?
(e) What function does the capacitor C1 serve?

Procedure 5 Common-emitter amplifier with bypassed emitter resistor

Set-Up

Keep the circuit of procedure 4 set up, as shown in Fig. E2.4, with the signal or function generator input applied to node BC and the output taken from node C. The oscilloscope Ch-1 input should be connected to the signal input on node BC, and Ch-2 should be connected to the output at node C. The power supply should still be set up to produce a +15 V rail relative to the Gnd (ground) rail. The oscilloscope and signal generator grounds should also remain connected to the Gnd rail.

Now, connect the free end of capacitor C2 (node EC) to ground to produce an emitter resistor bypass. Adjust the signal generator to produce a 1.0 kHz sinewave with a peak-to-peak amplitude of 100 mV. (This is a factor of 10 smaller than previously.)

Comment

The emitter resistor RE was used in procedure 3 to aid in stabilizing the bias of transistor Q1, making it less sensitive to variations in the transistor β. However, it also has the effect of lowering the voltage gain of the amplifier. The bias point only needs to be established for DC conditions, so if the amplifier is to be used for frequencies above DC, the emitter resistor can be bypassed for sufficiently high frequencies by shunting it with a capacitor. This is what is done when node EC is connected to ground. For DC, capacitor C2 is effectively an open-circuit, and RE stabilizes the bias point as before. For sufficiently high frequencies, the impedance of capacitor C2 falls to the point where the emitter of Q1 is effectively grounded.

Measurement-5

Turn the DC power supply ON, and adjust the oscilloscope to display both the input and output signals versus time. Ch-1 should be set to 100 mV/div, and Ch-2 should be set to 5 V/div. Adjust the sweep rate to 1 ms/div to display about 10 cycles of each sinewave.

Adjust the amplitude of the signal or function generator so that the output sinewave is as large as possible, but not yet clipping on either polarity peak. Calculate the voltage gain of the amplifier by dividing the amplitude of the output sinewave by the amplitude of the input sinewave and record the result in your lab notebook.

Increase the amplitude of the input sinewave from the signal or function generator until the output waveform just begins to clip at either the negative or positive peak. Record this clipping voltage in your lab notebook. Increase the amplitude of the input signal further until the output waveform clips on the the other polarity, and record this clipping level in your lab notebook.

As was done in the procedure 4, reduce the amplitude of the signal or function generator until the output sinewave is no longer clipped. Increase the frequency of the signal or function generator until the amplitude of the output sinewave has fallen to about 70 percent of its initial value at 1 kHz. This will probably occur around 1 MHz, so the oscilloscope and the input signal will need to have their time bases adjusted together to retain 5-20 complete cycles on the oscilloscope display. Record in your lab notebook the frequency at which the ratio of the output to input amplitude has fallen to the 70 percent point. This is the –3 dB bandwidth of this amplifier.

Question-5

(a) Is this amplifer inverting or non-inverting?
(b) How do the clipping points compare to those of the common-emitter amplifier without the emitter resistor bypass? Does the presence of the bypass capacitor affect the clipping levels?
(c) Calculate the frequency at which the impedance of the bypass capacitor is equal to the resistance of RE. Above this frequency, capacitor C2 forms an effective bypass for RE.
(d) What is the flat frequency response range for this amplifier?
(e) How does the –3 dB bandwidth of the bypassed common-emitter amplifier compare to the unbypassed case? Does the presence of the bypass capacitor have any effect on the high frequency characteristics?

Procedure 6 Common-collector amplifier (emitter-follower)

Comment

When the input signal is applied to the base terminal and the output signal taken from the emitter terminal, the collector terminal is thus common between the input and output ports, and the configuration is termed a common-collector amplifier stage. Since the voltage at the emitter essentially follows (tracks) the voltage at the base, this configuration is also called an emitter follower. Both names are synonymous and used equally.

Set-Up

Keep the circuit of procedure 4 or 5 set up, as shown in Fig. E2.4, with the signal or function generator input applied to node BC. The emitter resistor RE should not be bypassed; that is, node EC of capacitor C2 should remain unconnected. The power supply should still be set up to produce a +15 V rail relative to the Gnd (ground) rail. The oscilloscope and signal generator grounds should also remain connected to the Gnd rail. The Ch-1 oscilloscope input should still be taken from node BC, but the Ch-2 input should now be drawn directly from the emitter of Q1, node E.

Adjust the signal generator to produce a 1.0 kHz sinewave with a peak-to-peak amplitude of 1 V.

Measurement-6

Turn the DC power supply ON, and adjust the oscilloscope to display both the input and output signals versus time. Both Ch-1 and Ch-2 should be set to 5 V/div with DC coupling to observe where each is located within the rail-to-rail voltage span. To better observe the signals on each, change both Ch-1 and Ch-2 to 1 V/div and use AC coupling. Adjust the sweep rate to 1 ms/div to display about 10 cycles of each sinewave.

Adjust the amplitude of the signal or function generator so that the output sinewave is as large as possible, but not yet clipping on either polarity peak. Calculate the voltage gain of the amplifier by dividing the amplitude of the output sinewave by the amplitude of the input sinewave and record the result in your lab notebook.

Increase the amplitude of the input sinewave from the signal or function generator until the output waveform just begins to clip at either the negative or positive peak. Record this clipping voltage in your lab notebook. Increase the amplitude of the input signal further until the output waveform clips on the the other polarity, and record this clipping level in your lab notebook.

As was done in the procedure 4, reduce the amplitude of the signal or function generator until the output sinewave is no longer clipped. Increase the frequency of the signal or function generator until the amplitude of the output sinewave has fallen to about 70 percent of its initial value at 1 kHz. This will probably occur at a frequency in excess of 10 MHz, so it is possible that the signal generator will begin losing amplitude before the amplifier under test does. For this reason, it is important to take the ratio between the output and input amplitudes. Record in your lab notebook the frequency at which the amplitude *ratio* has fallen to the 70 percent point. This is the –3 dB bandwidth of this amplifier.

Question-6 (a) Is the common-collector amplifier inverting or non-inverting?
(b) Since the voltage gain of this amplifier is actually less than unity, what is the usefulness of this amplifier?

Procedure 7 Common-base amplifier

Comment

When the signal input is applied to the emitter terminal and the output drawn from the collector terminal, the base terminal is therefore common between the input and output ports, and the amplifier configuration is termed a common-base.

Set-Up

Keep the circuit of procedure 4, 5, or 6 set up, as shown in Fig. E2.4. Connect the output of the signal or function generator to the free end of capacitor C2, node EC. The base resistors R1 and R2 should be bypassed by connecting the free end of capacitor C1 to ground; that is, node BC of capacitor C1 should be connected to the ground rail. The power supply should still be set up to produce a +15 V rail relative to the Gnd (ground) rail. The oscilloscope and signal generator grounds should remain connected to the Gnd rail. The Ch-1 oscilloscope input should be taken from the signal input at node EC, and the Ch-2 input should be taken from the collector of Q1, node C.

Adjust the signal generator to produce a 1.0 kHz sinewave with a peak-to-peak amplitude of 100 mV.

Measurement-7

Turn the DC power supply ON, and adjust the oscilloscope to display both the input and output signals versus time. Ch-1 should be set to 100 mV/div, and Ch-2 should be set to 5 V/div. Adjust the sweep rate to 1 ms/div to display about 10 cycles of each sinewave.

Adjust the amplitude of the signal or function generator so that the output sinewave is as large as possible, but not yet clipping on either polarity peak. Calculate the voltage gain of the amplifier by dividing the amplitude of the output sinewave by the amplitude of the input sinewave and record the result in your lab notebook.

Increase the amplitude of the input sinewave from the signal or function generator until the output waveform just begins to clip at either the negative or positive peak. Record this clipping voltage in your lab notebook. Increase the amplitude of the input signal further until the output waveform clips on the the other polarity, and record this clipping level in your lab notebook.

As was done in the procedure 4, reduce the amplitude of the signal or function generator until the output sinewave is no longer clipped. Increase the frequency of the signal or function generator until the amplitude of the output sinewave has fallen to about 70 percent of its initial value at 1 kHz. This will probably occur at a frequency in excess of 1 MHz. Record in your lab notebook the frequency at which the amplitude *ratio* has fallen to the 70 percent point. This is the –3 dB bandwidth of this amplifier.

Question-7

(a) Is the common-base amplifier inverting or non-inverting?
(b) Speculate on the effect of not bypassing the base resistors R1 and R2. If you don't have any ideas, go ahead and try this in the lab if you have time.
(c) From the results of this lab experiment and those of experiment 1, explain why the base terminal of a BJT is never useful as an amplifier output.
(d) From the results of this lab experiment and those of experiment 1, explain why the collector terminal of a BJT is never useful as an amplifier input.