Experiment-3

JFET and MOSFET Characterization

Introduction

The objectives of this experiment are to observe the operating characteristics of junction field-effect transistors (JFETs) and metal-oxide-semiconductor field-effect transistors (MOSFETs). Some basic methods for extracting device parameters for circuit design and simulation purposes are also examined.

Precautions

Junction field-effect transistors (JFETs) involve only an internal pn-junction and are thus relatively static insensitive and may be handled freely. However, MOSFETs involve a very thin gate oxide layer which may not have any static protection diodes included as part of the device. As a result, MOSFETs can be very static sensitive and must be treated properly to avoid having to buy replacements.

To avoid static discharge damage to MOSFETs, keep their leads inserted into black conductive foam whenever possible. Always touch a grounded object, such as the frame of the lab bench, to discharge any built-up static charges from your body before handling the MOSFET. After this, carefully remove the MOSFET from the black foam and insert it into either the curve tracer or the solderless breadboard. Pay particular attention to correctly identifying the leads on the devices. Improper connection of the device is another means in which they can be destroyed. Once the MOSFET is correctly connected into its test circuit, it is reasonably well protected from static, since there now exist resistors or power supply terminals which allow current to flow from lead to lead. As a basic rule, remember that static electricity affects only floating terminals on a device or circuit. Simply connecting these floating terminals to ground with a large value resistor, say 1 MΩ or so, is often sufficient to provide a discharge path for any built-up charges.

If you are still having difficulty in keeping the MOSFETs from being destroyed by static, you may wish to try another trick which works well for very senstive parts. While the MOSFET is still plugged into the conductive black foam, take a 1-2 inch long piece of very fine bare copper wire and wrap it around all of the leads, just below the lip of the case, so that it shorts all of the leads together. (Some discrete MOSFETs even come with a piece of wire around the leads for this purpose.) Twist the free ends of the wire together so that it will not fall off. After the leads have all been shorted together by the wire, remove the MOSFET from the black foam and re-insert it into either the curve tracer or the solderless breadboard. Finish all of the rest of the circuit connections and instrument set-ups, and then only before you test the circuit, remove the bare copper shorting wire. Re-wrap the MOSFET leads with the bare copper shorting wire before removing it from the breadboard or test fixture.

Electrostatic discharge (ESD) can very frequently arise from a human body transferring a static electric charge to the circuit or device. The human body acts like a small capacitance relative to the Earth ground, and when discharged into a circuit, the current is limited by the tissue and skin impedance. The standard human body model (HBM) for electrostatic discharge simulation consists of a 100 pF capacitor in series with a 1.5 kΩ resistor. The 100 pF capacitor can become charged to fairly high voltages by comparatively simple actions, as shown in the following table, taken from the Motorola Power MOSFET Data Book:

Action	Electrostatic Voltage: 10-20 % rel. humid. (V)	Electrostatic Voltage: 65-90 % rel. humid. (V)
walking on carpet	35,000	1,500
walking on vinyl floor	12,000	250
working at a bench	6,000	100
handling a vinyl envelope	7,000	600
picking up a poly bag	20,000	1,200
shifting position in a chair	18,000	1,500

A relative humidity of 10-20 % is extremely dry (and almost never occurs in Seattle), while relative humidity in the range of 65-90 % is more typical for the Pacific Northwest. Thus, our ESD problems are quite tame compared to the situation in the dry Southwest of the United States.

MOSFET arrays are integrated circuits which contain several MOSFETs fabricated into a common silicon substrate. Most of the time, the gates of these MOSFETs are internally protected from ESD by clamping diodes to both the upper and lower power supply rails. If the voltage on the gate pin exceeds the upper power supply rail by V_{on}, then the upper clamp diode will turn on an keep the voltage from rising further. If the voltage on the gate pin falls below the lower power supply rail by V_{on}, then the lower clamp diode will turn on and keep the voltage from falling further. In this manner the input gate voltages are clamped within the range of $V_{SS} - V_{on}$ to $V_{DD} + V_{on}$. MOSFET arrays with internal clamping diodes are fairly safe to handle and are much more robust than individual discrete MOSFETs which have no gate protection. The CD4000 family CMOS logic integrated circuits used in this and the other experiments have these ESD input protection diodes.

Procedure 1 Discrete MOSFET gate lead, sex, and mode identification

Comment — The objective of this procedure is to learn how to identify the leads, the sex, and the mode of a MOSFET using only a digital multimeter (DMM). The method for achieving this is based upon looking for pn-junctions and insulating oxide layers between the different pairs of terminal leads. Thus, one should first become familiar with using a DMM to find these junctions.

Practice — Turn on a bench DMM and configure it to measure (two wire) resistance. Plug a black squeeze-hook test lead into the negative banana jack of the meter and a red squeeze-hook test lead into the positive banana jack of the meter. Locate a 1N4148 diode from the parts kit and measure its resistance with the DMM in both the forward and reverse bias directions. Note that the red lead from the positive input of the DMM is the one which will have the more positive voltage for this test. Record these readings in your lab notebook, and note these readings as being typical for a forward and reverse biased pn-junction. You can then refer to these readings to determine the polarity of pn-junctions that exist between pairs of leads of a MOSFET.

Comment — Most modern DMMs perform resistance measurements with a very small test voltage, in order to minimize battery drain. As a result, this test voltage may be insufficient to turn on a pn-junction, rendering the meter useless for this application. Many modern DMMs offer a special range position as part of the resistance mode which uses a larger test voltage of 1.5 to 2.5 V to turn on a given pn-junction diode. More advanced DMMs have a diode test position which displays the diode's forward turn-on voltage when a current of a few mA is passed through it. This range is usually indicated by a small diode symbol on the selector switch. When the pn-junction is forward biased, the meter will read the diode's turn-on voltage, while when reverse biased, the meter will read the open-circuit test voltage across the diode, which is usually 2.0 V or greater. Hence, in a diode test mode, the larger voltage reading indicates the reverse-bias polarity of the diode, while a forward-bias polarity of the diode would be indicated by a typical turn-on voltage of about 0.6 Volts or so.

Practice — Next, if your DMM has this feature, select the diode test function on the DMM, as identified by the small diode symbol next to it. Measure the voltage across the 1N4148 diode when forward and reverse biased, and record these in your laboratory notebook as typical values. These readings will help you to identify pn-junctions in other devices.

Comment — Very old volt-ohm-ammeters (VOMs), such as the classic model 206 Simpson and other D'Arsonval movement meters (those with a mechanical needle and scale), usually implemented the ohms function with an internal 1.5 V battery which made the red lead more *negative* than the black lead. As a result, when

using one of these meters to determine diode polarities, one must mentally reverse the lead polarities in order to obtain the correct deductions from the readings. On most modern DMMs, including handhelds, the red and black leads *do* have the correct voltage polarity in the ohms mode, i.e. red being more positive than black.

Set-Up

Locate a type 2N7000 MOSFET from the parts kit. This should be a three lead device in a small plastic TO-92 package. Insert the device into a solderless breadboard; this will help keep the part positioned while the various lead combinations are probed with the DMM test leads. You might find that a few short jumper wires are also useful for quickly connecting the device to the DMM test leads. The objective of this procedure will be to determine as much information as possible about an "unknown" MOSFET, using only simple DMM measurements.

Measurement-1

The gate lead of a MOSFET is separated from the other leads by the gate oxide layer which forms the gate of a MOS capacitor. For DC, this capacitor should not pass any current. Thus, use the DMM in the resistance mode to find the lead on the 2N7000 MOSFET which does not conduct to any of the other leads, in either polarity.

With the gate lead identified, it stands to reason that the remaining leads must be the drain and the source. The 2N7000 MOSFET happens to have a special internal diode which guards against the drain being taken more negative than the source, as shown in Fig. E3.1. (This situation can occur during transient switching of an inductive load, and the internal diode is present to protect against this.) The body of the MOSFET is also internally connected to the source lead, effectively making the four terminal MOSFET a three terminal part.

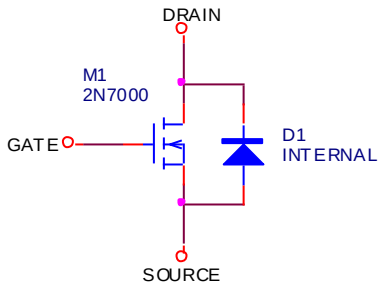

Figure E3.1

Switch the DMM to the diode test function and determine the source and drain leads from the direction that the transient protection diode allows current to pass (from source to drain). For the 2N7000 MOSFET, this also verifies that it is an n-channel device.

More conventional MOSFETs which do not have either the transient protection diode or their body and source tied together (a true four-terminal MOSFET) would show the source and drain as symmetrical in so far as any DMM measurements are concerned. For such devices, the polarity of the body diode would be used to identify the body terminal and also whether the MOSFET was n-channel or p-channel.

With all three leads of the 2N7000 MOSFET now identified, short the gate and source leads together with a small jumper wire on the solderless breadboard. This is to guarantee that $V_{GS} = 0$. Use the DMM to measure the conduction from drain to source. If this is significant, then the device channel is turned on without any gate bias, and the MOSFET is a depletion mode (D-mode) or "normally-ON." If the conduction from drain to source with $V_{GS} = 0$ is negligible, then the MOSFET is an enhancement mode (E-mode) or "normally-OFF." Make this determination for the 2N7000 MOSFET and record the results in your laboratory notebook.

Question-1

(a) From your measurements above, summarize your findings about the given 2N7000 MOSFET in your notebook.
(b) Draw a picture of the device package and label the leads. (It is conventional to do this with a view of the device looking down on it with the leads pointing away from you, as if it were soldered into a printed circuit board. This is usually termed a component-side view, in reference to the component side of the circuit board.)
(c) Look up the data sheet for the the 2N7000 and compare your deductions with the manufacturer's specifications. (Data sheets can be most easily obtained online from the EE Stores web pages.) Comment on any discrepancies.
(d) Draw up a flow chart for testing any four-terminal MOSFET with an ohmmeter which can be used to conclusively determine which lead is the gate, which lead is the body, whether the device is an n-channel or p-channel, and whether the device is a D-mode or an E-mode.
(e) If the gate oxide were destroyed by a static electricity discharge, speculate on how the DMM readings might be different from those that were observed.

Extra Fun

Because the gate lead on the 2N7000 MOSFET is "naked," i.e. not connected to any other junctions or any ESD protection diodes, it can be charged up by the momentary application of a DC voltage, and the MOS gate oxide capacitance will hold this charge for a fairly long period of time. The voltage used for the diode test function of a DMM is sufficiently high to turn on the channel of the 2N7000 MOSFET, so this can be used to check its operation. If the DMM does not have a diode test function, then this procedure will not work, because the regular test voltage used for measuring resistance will be insufficient to turn on the MOSFET. In other words, the test voltage is less than the threshold voltage V_T of the MOSFET.

Remove the small jumper wire that was shorting the gate to the source, and switch the DMM to the diode test function mode. Touch the positive, red DMM lead to the gate and the negative, black DMM lead to the source. This will charge up the gate capacitor with a $V_{GS} > 0$. Now measure the conduction between the drain and the source, and you should observe a conducting channel. Next, touch the negative, black DMM lead to the gate and the positive, red DMM lead to the source. This will discharge the gate capacitor, making $V_{GS} < 0$, and turn the channel back off again. Verify this by measuring the channel conduction again. There should be a significant difference in channel conductance between the conducting and non-conducting states.

Procedure 2 Integrated MOSFET lead, sex, and mode identification

Comment

This procedure will use the CD4007 CMOS integrated circuit. This is a very general purpose CMOS IC which includes an array of 3 n-channel and 3 p-channel MOSFET's connected as shown in Fig. E3.2a. The digits by each terminal indicate the pin numbers on the 14-pin DIP package, shown in Fig. E3.2b. Note that pin 14 (VDD) must *always* be connected to the most positive power supply voltage, and pin 7 (VSS) must *always* be connected to the most negative (or ground) power supply voltage in order to keep the body-source and body-drain pn-junctions from becoming forward biased. This is what provides electrical isolation between the different MOSFETs in the integrated circuit, and if this isolation fails, all of the MOSFETs end up being shorted together with completely unpredictable results. Although it is not shown in the schematic, each of the three inputs to the MOSFET gates (pins 3, 6, & 10) have two ESD protection diodes that connect them to the VDD and VSS power rails.

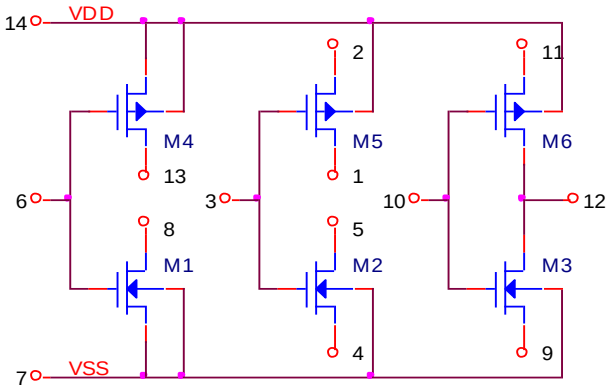

Figure E3.2a

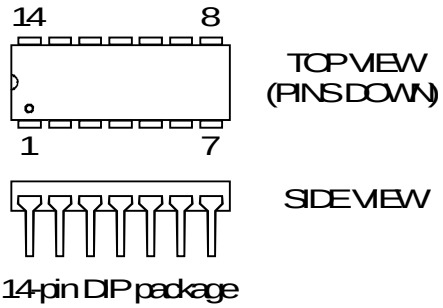

Figure E3.2b

Set-Up

Locate the CD4007 CMOS array integrated circuit. Plug the CD4007 into the solderless breadboard so that it straddles the center groove. This procedure will perform tests only on MOSFET M2 in Figure E3.2a. You may find it helpful to plug short jumper wires into the solderless breadboard to contact pins {3,4,5,7, & 14} of the integrated circuit. All of the next measurements will involve only these leads.

Turn on a bench DMM and configure it to measure resistance in a two wire mode. Plug a black squeeze-hook test lead into the negative banana jack of the meter and a red squeeze-hook test lead into the positive banana jack of the meter. The objective of this procedure will be to verify the leads, sex, and mode of the MOSFET using only the ohmmeter function of the DMM.

Measurement-2 Consider only pins {3,4,5, & 7} of the IC which connect to the {G,S,D & B} of MOSFET M2. First, the identification of these leads will be verified. A MOSFET gate is normally completely isolated from the other electrodes by a thin insulating layer of silicon dioxide. On a discrete MOSFET that has no internal gate protection diodes, a DMM in its ohmmeter setting can be used to first find the gate lead as the one which does not have conduction to any other lead in either polarity. For the CD4007 CMOS array, the presence of the internal gate protection diodes complicates the problem of identifying the gate lead. For this situation, it is usually easier to identify the body lead first. Because of the presence of the ESD protection diodes on the gate, the body at VSS will conduct to the gate through one diode, and the gate will conduct to the upper VDD rail through the other diode. However, the body terminal is unique, because it will exhibit conduction from the body to each of the other three terminals when the body is the more positive terminal. Probe different pairs of leads (pins 3,4,5, & 7) with the DMM to find the one pin which conducts (like a forward biased pn-junction) to each of the other three. Since this corresponds to current going into the body terminal, this also verifies that the MOSFET is an n-channel, since its body must be p-type for this to occur.

With the body lead identified, the gate lead can then be identified next, because of the electrical symmetry between the drain and source. Because the voltage used by the DMM in the diode test function can easily turn on the MOSFET channel, the best method to identify the gate is to find the terminal which, when shorted to the body with a jumper, causes the other two terminals to show symmetric electrical behavior. That means that when the gate is shorted to the body, the channel of the MOSFET should be non-conducting, and the only conduction involving the source and drain should be through the source-body and drain-body pn-junctions. Test the MOSFET M2 with the DMM and a short jumper wire to identify the gate in this manner.

With the gate and body leads identified, the remaining two leads must therefore be the drain and source. Now use the DMM, again in its ohmmeter setting, to determine whether the device is a depletion-mode (D-mode, or normally-ON) or an enhancement-mode (E-mode, or normally-OFF) device. Because the gate could have picked up a stray charge that has not fully dissipated, one must insure that the gate bias is at zero. This is done by using a small jumper wire to short the gate to the body, giving $V_{GB} = 0$, similar to the connection used previously to identify the gate lead.

As mentioned, the gate of MOSFET M2 has two ESD protection diodes, one to VDD and the other to VSS. If the gate (pin 3) is taken to a voltage higher than VDD (pin 14), then the ESD protection diode between the two will turn on, clamping the voltage difference to the diode turn-on voltage. Use the DMM in the diode test function to verify the presence of the ESD protection diode between the gate and VDD.

Question-2

(a) From your measurements above, summarize your findings about MOSFET M2 in your notebook.
(b) Draw a schematic of MOSFET M2 and its two gate protection diodes and label the MOSFET leads.
(c) Is it possible to distinguish the drain lead from the source lead using only an ohmmeter? Explain why or why not.
(d) If the power leads to the CD4007 IC are reversed, with VSS at a higher potential than VDD, then other pn-junction diodes can be turned on, clamping this voltage to the diode turn-on voltage. Using the schematic of Fig. E3.2a, show how current can flow from VSS to VDD and create a voltage drop of <u>two</u> diode turn-on voltages (about 1.2 V).
(e) If the connection between MOSFETs M3 and M6 were broken (through their drains at pin 12), conduction from VSS (pin 7) to VDD (pin 14) would still occur, but it would involve only <u>one</u> diode turn-on voltage (about 0.6 V). Explain how this occurs. This is, in fact, what happens when you measure it. Because this path involving only one diode turn-on voltage happens at a smaller voltage, the path involving two diode turn-on voltages in series never gets activated.

Procedure 3 Measurement of a MOSFET using a LabVIEW curve tracer

Comment

To characterize a multi-lead semiconductor device such as a MOSFET, we would like to be able to know and predict the currents through each lead as a function of the voltages between each of the leads. Since the gate lead does not allow any DC current to pass, and the body will be non-conducting when the body diodes are reverse-biased, the only current to consider in a normally functioning MOSFET is the channel current flowing from drain to source, I_D. But this is still a function of the three terminal voltages, V_{GS}, V_{DS}, and V_{BS}. The V_{BS} dependence is the weakest, and we shall suppress it for the time being by keeping $V_{BS} = 0$. The normal manner for displaying the characteristics of the MOSFET involving I_D as a function of V_{GS} and V_{DS} is to plot several curves of I_D versus V_{DS} on these axes for selected values of V_{GS}. These are termed the output characteristics. The other way is to plot I_D versus V_{GS} on these axes for selected values of V_{DS}. These are termed the transfer characteristics. The objective of this procedure will be to measure and record the output characteristics of a MOSFET using an automated LabVIEW curve tracer.

Set-Up

First, copy the LabVIEW VI files to a directory on your laboratory computer. Then, launch LabVIEW and open the VI named FETCurveTracer.vi. This is the main VI that will be used for this procedure, but it uses two other sub-VIs, named FETStepGenerator.vi and FETMeasurement.vi which must be in the same directory as the FETCurveTracer.vi. Once you have the FETCurveTracer.vi open, the front panel should appear as shown in Fig. E3.3 below:

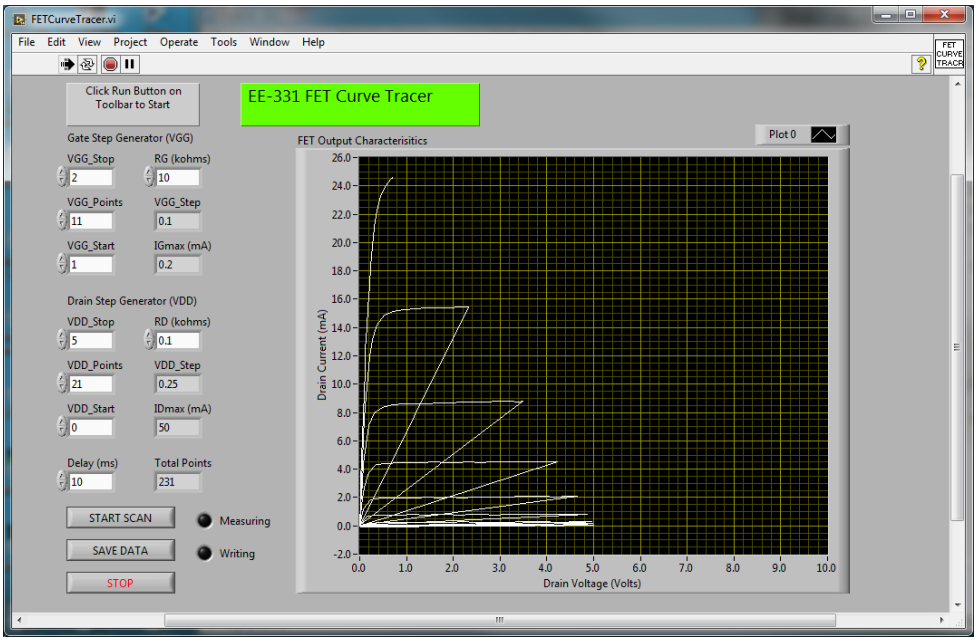

Figure E3.3

Similar to the diode curve tracer of Experiment-1, this FET curve tracer also operates by scanning an excitation voltage that is applied across a series connection of the device under test (DUT) and a current sampling resistor. The voltages across both the DUT and current sampling resistor are measured by the DAQ hardware, and from this, a current-voltage (I-V) point is measured for the device. However, for the FET curve tracer, there are now <u>two</u> excitation voltages, VGG and VDD, which are applied to the gate and drain circuits, respectively, while the source of the FET is kept grounded. In order to scan through all of the combinations of possible V_{GS} and V_{DS} values, the VDD scan is nested within the VGG scan. For each value of VGG, all of the VDD values are scanned in sequence, giving a total number of measurement points which is the product of the number of VGG and VDD points. As can be seen from the output characteristics shown in Fig. E3.3, for each VGG value, the VDD values scan outward from the origin to their final value, and then the next VGG value is used to scan outward again. This creates the straight retrace lines that are shown in Fig. E3.3, coming out radially from the origin. These are merely an artifact of the scanning sequence, and do not affect the measured data.

The LabVIEW VI is designed to use a National Instruments NI-USB-6009 DAQ. All four differential analog inputs and both analog outputs are used to implement the FET curve tracer. All of these terminals are on the analog connector block of the DAQ, pins 1-16. The overall connections are shown in the schematic of Fig. E3.3a, with the pin numbers shown for each terminal.

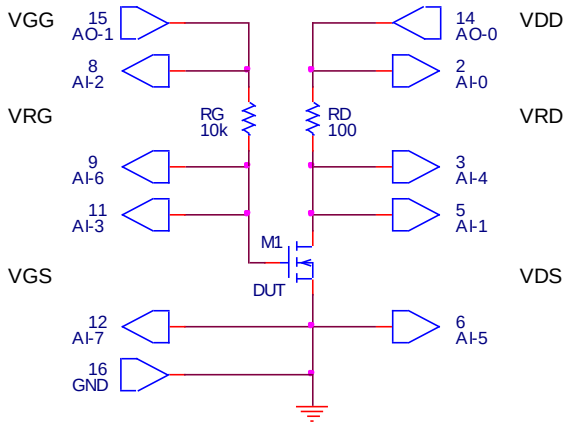

Figure E3.3a

The excitation voltage VDD is taken from the analog output channel-0 (AO-0) which uses pin #14 for AO-0 and pin #16 for the analog output ground (GND). Note that all of the pins labeled GND on the DAQ are equivalent (pins #1, 4, 7, 10, 13, and 16). The VDD voltage is applied across the series connection of a drain current sensing resistor RD = 100 Ω, and the drain-source leads of the device under test (DUT). Thus, VDD = VRD + VDS. Similarly, the excitation voltage VGG is taken from the analog output channel-1 (AO-1) which uses pin #15 for AO-1 and pin #16 for GND. The

voltage is applied across the series connection of a gate current sensing resistor RG = 10 kΩ, and gate-source leads of the DUT. Thus, VGG = VRG + VGS. Under normal conditions, no DC gate current should flow in the DUT, and so the voltage drop across RG should be zero, giving VGS = VGG. The purpose of RG is primarily to serve as a safety device that would limit excessive currents should a short circuit occur in the DUT. It is generally good engineering practice to include current limiting safety resistors like this.

Each of the four analog inputs uses a differential mode connection, so that the measured voltage is the difference between the voltages on each pair of analog input leads. VRD is measured using analog input channel-0 (AI-0), which takes the difference between AI-0 (pin #2) and AI-4 (pin #3). VDS is measured using analog input channel-1 (AI-1), which takes the difference between AI-1 (pin #5) and AI-5 (pin #6). VRG is measured using analog input channel-2 (AI-2), which takes the difference between AI-2 (pin #8) and AI-6 (pin #9). VGS is measured using analog input channel-3 (AI-3), which takes the difference between AI-3 (pin #11) and AI-7 (pin #12). Finally, the analog ground (GND) on pin #16 is connected to the source of the DUT. Any of the other GND pins could also work for this.

The best approach to constructing the circuit of Fig. E3.3a is to place as many as possible of the connections on the DAQ analog connector block itself, along with the current sensing resistors RD and RG, and then take the DUT connections off of the connector block to a solderless breadboard using three longer jumper wires. This will reduce the number of wires that need to go between the DAQ and the solderless breadboard, and also make it easier to switch around the DUT connections for different devices. Figure E3.3b shows one way of making these connections. The gate circuit uses the green wire; the drain circuit uses the red wire, and the grounded source uses the black wire. These connection now effectively make the NI-USB-6009 into a three-terminal FET curve tracer.

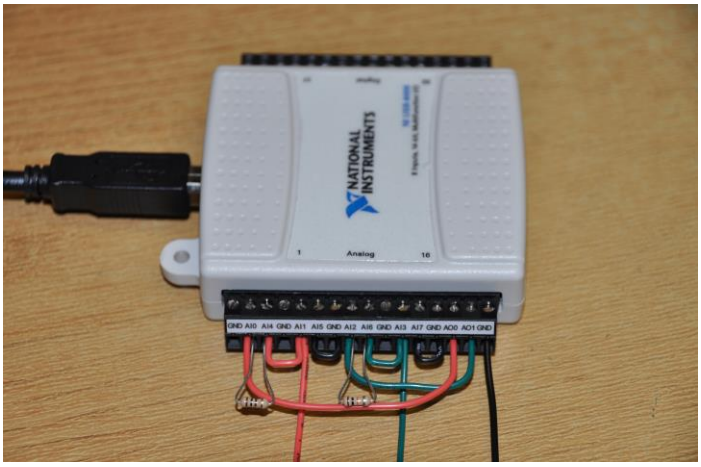

Figure E3.3b

Next, locate the 2N7000 MOSFET that was used in Procedure 2, and insert it into the solderless breadboard. Connect the source (black), gate (green), and drain (red) leads from the DAQ analog connector block to the 2N7000 MOSFET as shown in Fig. E3.3c. The device is now ready to measure.

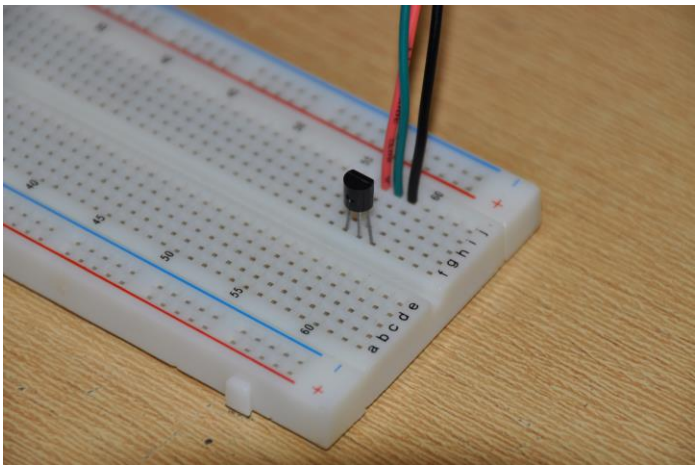

Figure E3.3c

Measurement-3 Start the LabVIEW FETCurveTracer.vi by clicking on the Run button on the toolbar. Use the index finger pointer to input the scan parameters as follows. Input the current sensing resistor values as RG = 10 kΩ and RD = 0.1 kΩ. Set the Delay = 10 (ms). Since the threshold voltage for the 2N7000 MOSFET is anticipated to be in the range of 1-2 Volts, set the VGG scan to start at 1.0 V, stop at 2.0 V, and use 11 points, giving +0.1 V/step. Set the VDD scan to start at 0.0 V, stop at +5.0 V, and use 21 points, giving +0.25 V/step. There should be a total of 231 measurement points. After all of the scan parameters have been entered, click on the START SCAN button. The red Measuring LED should glow while the data is being taken. After all of the data points have been collected, the resulting output characteristics will appear on the graph, similar to that shown in Fig. E3.3.

To store the results in a spreadsheet file, click on the SAVE DATA button, and a dialog box will open, allowing you to specify the filename of the Excel .xls file and its location. Enter a filename like Experiment_3_Procedure_3 _2N7000.xls, and click on OK. The spreadsheet file will be written, and the red Writing LED will extinguish. After the data has been saved to a spreadsheet file, halt the running VI by clicking on the red STOP button.

Open up the spreadsheet file that was just written and examine the contents. There should be 8 columns of data, with a measurement point on each row. The columns are, reading left to right: {VGG, VDD, VRD, VDS, VRG, VGS, IDS, & IGS}. You might wish to insert a column header row to indicate this for future reference, since the LabVIEW VI does not insert these column labels. The first two columns are just the two excitation voltages VGG and VDD which were sent to the DAQ analog output channels. The next four

columns are the analog input channel measurements, {VRD, VDS, VRG, & VGS}. The last two columns are the drain and gate currents which are computed as IDS = VRD/RD and IGS = VRG/RG. You should find that the gate current is zero for all of the data points and that the values of VGG = VGS, to within the LSB of the DAQ measurement channel (a few mV).

Question-3

(a) Scan through the measurement results and find the value of V_{GS} which just starts to produce a non-zero drain current. This is a first approximation to the threshold voltage V_T of the MOSFET under test.
(b) Pick a few values of V_{GS} for which the drain current I_D shows a clearly defined saturation. Find the value of V_{DS} at which the drain current I_D reaches its saturation value and then compare this actual value of $V_{DS,sat}$ to a computed value of $V_{GS} - V_T$. Comment on how close these values agree. How well does the textbook theory predict the measured behavior of a real MOSFET?
(c) Using an electron mobility value of $\mu_n = 800$ cm^2/V-s and a gate oxide thickness of $x_{ox} = 80$ nm, compute the value of $k = \mu_n C_{ox}$, and from this value and a few of the measured data points (where the drain current is saturated) make a rough estimate of the W/L ratio for the 2N7000 MOSFET. Does this W/L ratio seem reasonable?

Comment

At some of the larger values of VGG = VGS, the spreadsheet data may show that VRD + VDS does not equal the applied VDD value. This is because the current output of the DAQ is limited to only 10 mA. Even though the software is telling the DAQ to output a certain value of VDD, the value will be less than this if the current were to exceed the 10 mA limit. Thus, the actual value of VDD drops back to a value which limits the current to no more than about 10 mA, and the resulting sum of VRD and VDS is then less than the original scan value of VDD at that measurement point. The measurement point data is still valid; the effect is only that the scan did not go as far out as originally intended. This can be seen on the front panel output characteristics graph, too.

The connector block wiring of Figs. E3.3a and E3.3b can be kept intact for the remaining parts of this experiment; there is no need to disassemble it now.

You may wish to investigate the internal workings of this LabVIEW VI. Type Ctrl+E to open the block diagram window, and you will see that the overall structure of this VI is fairly similar to that of the diode curve tracer used in Experiment-1. Locate the sub-VI named FETMeasurement.vi and double click on it to open up its front panel. Now type Ctrl+E again to display its block diagram. Each measurement point consists of a flat sequence of 7 steps. You can page through the steps to see what occurs during each. This is the core measurement sequence that is the heart of this VI.

Procedure 4 Measurement of CMOS pairs using a LabVIEW curve tracer

Comment

The objective of this procedure is to measure the characteristics of complementary n-channel and p-channel MOSFETs (CMOS), observe how well the n-channel and p-channel devices are matched in their parameters, and to gain further experience in measuring and characterizing MOSFETs that are part of an integrated circuit.

Set-Up-n

The LabVIEW FETCurveTracer.vi can be kept loaded from where it was left in Procedure 3, and no changes need to be made to the analog connector block wiring. Insert a CD4007 CMOS MOSFET array into a solderless breadboard and connect the gate, source, drain, and body leads to the n-channel MOSFET M2 (pins 3,4,5, & 7, respectively). Use long jumper wires to go from the connector block to the solderless breadboard. Refer to Figs. E3.2a and E3.2b for the correct pins on the IC. You will also need to use a small jumper wire to connect the body to the source, pins 4 and 7, which will set $V_{BS} = 0$. The final connections on the solderless breadboard are shown below in Fig. E3.4n. In this photo, the source lead is black, the gate lead is green, and the drain lead is red.

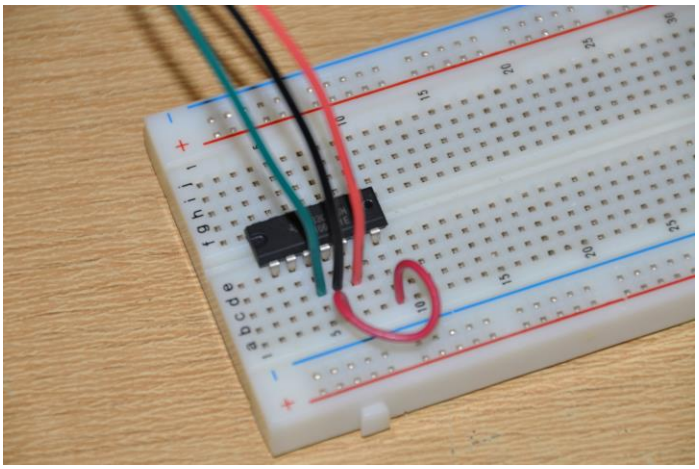

Figure E3.4n

Measurement-4n

Start the LabVIEW FETCurveTracer.vi and enter the following scan parameters: RG = 10 kΩ, RD = 0.1 kΩ, Delay = 10 (ms). Set the VGG scan to start at 0.0 V, stop at +5.0 V, and use 11 points, giving +0.5 V/step. Set the VDD scan to start at 0.0 V, stop at +5.0 V, and use 21 points, giving +0.25 V/step. This will give a total of 231 measurement points.

Click on the START SCAN button and wait for the measurement data to appear on the graph. If the data appears reasonable, click on the SAVE DATA button to record the measurements into a spreadsheet file. Give the new file a unique name and click on OK. Click on the red STOP button to halt the VI.

Open up the spreadsheet file and check that the data looks reasonable. The order of the columns is again, from left to right: {VGG, VDD, VRD, VDS, VRG, VGS, IDS, IGS}.

Question-4n

(a) Find the first value of V_{GS} which produces a non-zero drain current. This is a quick approximation to the threshold voltage V_{Tn} for the MOSFET. This should be a positive number for an n-channel E-mode MOSFET.
(b) Using values of μ_n = 800 cm^2/V-s and x_{ox} = 80 nm, compute the value of $k_n = \mu_n C_{ox}$. Next, select a value of V_{GS} which produces a clearly defined saturation of the drain current, and within the saturated range of this curve, use the value of k_n and V_{Tn} to find the effective W/L ratio for this MOSFET.

NOTE!!!

Because the NI-USB-6009 DAQ analog outputs cannot generate negative voltages, the p-channel part of this procedure cannot be easily performed. Stop here for now. A future laboratory handbook revision will repair this problem. The remaining p-channel measurements are left here simply for reference purposes.

Set-Up-p

Now move the drain, source, gate, and body jumper wires to pins (1, 2, 3, & 14, respectively) on the CD4007 CMOS MOSFET array IC to connect the curve tracer to the p-channel MOSFET M5. Again, refer to Figs. E3.2a and E3.2b for the correct pins on the IC. You will again need to use a small jumper wire to connect the source to the body, pins 2 and 14, which will set V_{BS} = 0. The final connections on the solderless breadboard are shown below in Fig. E3.4p. As before, the source lead is black, the gate lead is green, and the drain lead is red.

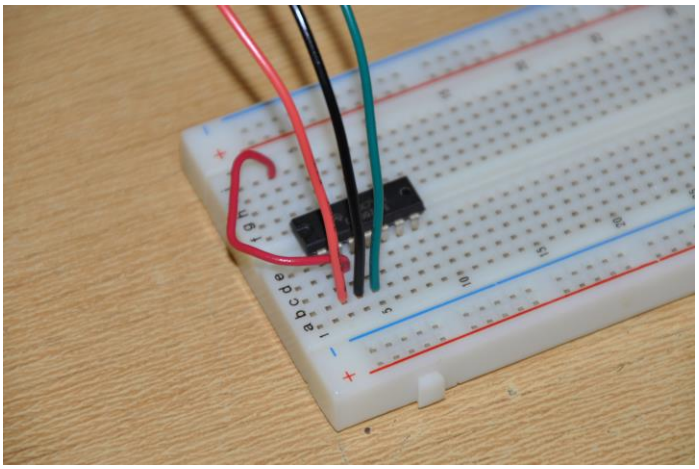

Figure E3.4p

Measurement-4p

With the LabVIEW FETCurveTracer.vi still loaded from the previous measurement, start the VI running, and keep all of the parameters in their previous settings. Now simply change the sign of the VGG and VDD stop values to negative numbers. The VGG scan should now start at 0.0 V, stop at –5.0 V, use 11 points, and give –0.5 V/step. The VDD scan should now start

at 0.0 V, stop at –5.0 V, use 21 points, and give –0.25 V/step. There should again be 231 total measurement points.

Click on the START SCAN button and wait for the measurement data to appear on the graph. You may have to right click on the graph and select Autoscale X Axis, since the data will now be appearing in the 3rd quadrant. (The 3rd quadrant is the more technically correct way to display p-channel FET characteristics. Even so, some data books choose to rotate the curves into the 1st quadrant for better readability while reversing the signs on the axes.) If the data appears reasonable, click on the SAVE DATA button to record the measurements into a spreadsheet file. Give the new file a unique name and click on OK. Click on the red STOP button to halt the VI. Open up the spreadsheet file and check that the data looks reasonable.

Question-4p

(a) Find the first value of V_{GS} which produces a non-zero drain current. This is a quick approximation to the threshold voltage V_{Tp} for the MOSFET. For a p-channel MOSFET, this should be a negative number for an E-mode device.
(b) Using values of $\mu_p = 320$ cm^2/V-s and $x_{ox} = 80$ nm, compute the value of $k_p = \mu_p C_{ox}$. Next, select a value of V_{GS} which produces a clearly defined saturation of the drain current, and within the saturated range of this curve, use the value of k_p and V_{Tp} to find the effective W/L ratio for this MOSFET.
(c) Compare the magnitudes of the threshold voltages for n-channel and p-channel MOSFETs and comment on how close they appear to be in practice.
(d) Compare the effective W/L ratios for the n-channel and p-channel MOSFETs and comment on what the ideal ratio between n-channel and p-channel devices should be in order to produce symmetrical I-V characteristics.

Procedure 5 Output conductance effects

Set-Up

Keep the CD4007 CMOS MOSFET array plugged into the solderless breadboard, but change its connections back to the n-channel MOSFET M2 on pins 3,4,5, & 7. A small jumper wire should again be used to short the body and source terminals together (pins 4 and 7). The final connections should look like those in the photo of Fig. E3.4n of the previous procedure.

Measurement-5

Start the LabVIEW FETCurveTracer.vi and enter the following scan parameters: RG = 10 kΩ, RD = 0.1 kΩ, Delay = 10 (ms). Set the VGG scan to start at 0.0 V, stop at +5.0 V, and use 11 points, giving +0.5 V/step. Set the VDD scan to start at 0.0 V, stop at +5.0 V, and use 21 points, giving +0.25 V/step. This will give a total of 231 measurement points.

Click on the START SCAN button and wait for the measurement data to appear on the graph. If the data appears reasonable, click on the SAVE DATA button to record the measurements into a spreadsheet file. Give the new file a unique name and click on OK.

Next, locate a 10 kΩ 5% 1/4 W resistor, and connect this resistor in parallel with the drain and source terminals of the MOSFET on the solderless breadboard (pins 4 & 5). This resistor simulates the effect of increasing the output conductance of the MOSFET. Click the START SCAN button again and wait for the measurement data to appear on the graph. If the data appears reasonable, click on the SAVE DATA button to record the measurements into a spreadsheet file. Give the new file a unique name and click on OK. Click on the red STOP button to halt the VI.

Question-5

(a) First discuss qualitatively what effect the addition of the 10 kΩ resistor has on the MOSFET output characteristics.
(b) Open the spreadsheet file for the first measurement of MOSFET M2 without the resistor being present, and select a value of V_{GS} which shows a clean saturation of the drain current. Select a few points within the saturated region of the curve and calculate the slope of the output characteristics in units of Ω^{-1}. Then take the reciprocal of this value to obtain the inverse slope in units of Ω. These values are the output conductance and resistance, respectively.
(c) Next open the spreadsheet file for the second measurement of MOSFET M2 with the resistor added, and perform the same analysis on the same V_{GS} curve to find the output conductance and resistance for this case.
(d) Discuss how closely these measured values match to the empirical device equation

$$I_{Dsat} = 0.5\ k(V_{GS} - V_T)^2\ (1 + \lambda V_{DS})$$

where λ is the output conductance parameter in units of V^{-1}.

Procedure 6 JFET gate lead, sex, and mode identification

Set-Up

Locate a type MPF102 JFET from the parts kit. This should be a three lead device in a small plastic TO-92 package. Turn on a bench DMM and configure it to measure (two wire) resistance. Plug a black squeeze-hook test lead into the negative banana jack of the meter and a red squeeze-hook test lead into the positive banana jack of the meter. The objective of this procedure will be to determine which lead of the JFET is the gate, whether the JFET is an n-channel or p-channel, and whether the JFET is an E-mode or D-mode device using only the ohmmeter function of the DMM.

Measurement-6

A JFET uses a single pn-junction between the gate and the drain/source terminals to modulate the channel conductance. Use the DMM in its ohmmeter setting to test pairs of leads on the JFET and therefore identify the gate lead on the device. From the polarity which causes the gate terminal to conduct, deduce whether the JFET is an n-channel or p-channel device.

With the gate lead identified, it stands to reason that the remaining leads must be the drain and the source. Use the DMM, again in its ohmmeter setting, to determine whether the device is a depletion-mode (D-mode, or normally-ON) or an enhancement-mode (E-mode, or normally-OFF) device.

Question-6

(a) From your measurements above, summarize your findings about the given MPF102 JFET in your notebook.
(b) Draw a picture of the device package and label the leads.
(c) Is it possible to distinguish the drain lead from the source lead using only an ohmmeter? Explain why or why not.
(d) Look up the data sheet for the the MPF102 and compare your deductions with the manufacturer's specifications. (MPF102 is a Motorola part number, but it is also second sourced by Fairchild.) Comment on any discrepancies.
(e) Draw up a flow chart for testing any JFET with an ohmmeter which can be used to conclusively determine which lead is the gate, whether the device is an n-channel or p-channel, and whether the device is a D-mode or an E-mode.

Procedure 7 Measurement of a JFET using a LabVIEW curve tracer

Set-Up

Load the LabVIEW FETCurveTracer.vi into LabVIEW, if it is not already. The DAQ analog connector block should be in the same configuration shown in Figs. E3.3a and E3.3b that was used for the previous curve tracer measurements. Locate an MPF102 JFET and plug it into the solderless breadboard. Connect the solderless breadboard to the connector block using jumper wires for the source, gate, and drain. The final connections on the solderless breadboard should look like those shown in Fig. E3.7 below. In this photo, the source lead is black, the gate lead is green, and the drain lead is red.

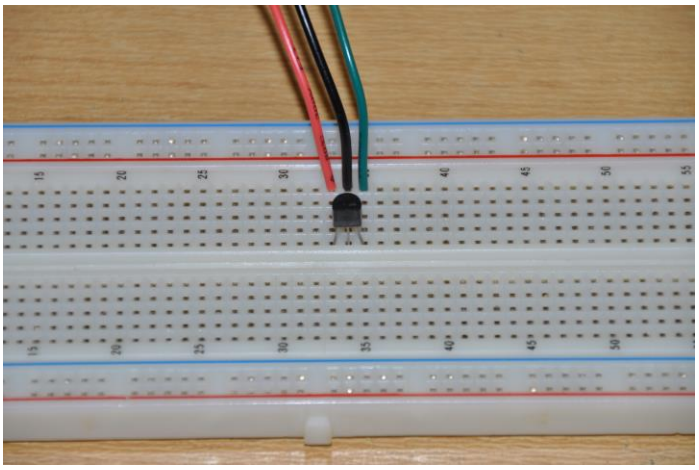

Figure E3.7

Measurement-7

Start the LabVIEW FETCurveTracer.vi and enter the following scan parameters: RG = 10 kΩ, RD = 0.1 kΩ, Delay = 10 (ms). Set the VGG scan to start at 0.0 V, stop at +0.5 V, and use 3 points, giving –0.25 V/step. This slightly forward biases the gate, which is all that the current NI-USB-6009 DAQ can do with only positive analog outputs. If it were possible, the curve tracer should ideally be programmed to scan over negative gate bias voltages. Set the VDD scan to start at 0.0 V, stop at +5.0 V, and use 21 points, giving +0.25 V/step. This will give a total of 63 measurement points, adequate for characterizing the JFET.

Click on the START SCAN button and wait for the measurement data to appear on the graph. If the data appears reasonable, click on the SAVE DATA button to record the measurements into a spreadsheet file. Give the new file a unique name and click on OK.

Now, swap the drain and source jumper wires (red and black leads in Fig. E3.7) and click on START SCAN to measure the device again with its drain and source interchanged. Save this data to another spreadsheet file with a new name. Click on the red STOP button to halt the VI.

Question-7 (a) From your results above, discuss the interchangeability of the drain and source leads on a JFET.
(b) From either spreadsheet file, scan the values of V_{GS} to find the value of the threshold voltage V_T for the JFET. If the values of V_{GS} are too coarsely spaced, you can create a quick graph of $I_{D,sat}$ versus V_{GS} in Excel to find a better graphical interpolation to the threshold voltage.
(c) From the spreadsheet data, find the value of saturated drain current that corresponds to a value of $V_{GS} = 0$. This is value is normally called I_{DSS}.
(d) Compare the theoretical values of $I_{Dsat} = I_{DSS} (1 - V_{GS} / V_T)^2$ to those recorded from the curve tracer in the spreadsheet. How close does this theoretical equation predict the actual device behavior?

Procedure 8 JFET variable attenuator

Comment

For small values of V_{DS}, the channel of a JFET or MOSFET behaves like a voltage-controlled resistor which can be utilized in many circuit applications where electronic control of a conductance or resistance is required. This is a more subtle use of the device than for the switching functions that it normally performs. The "on" resistance of the JFET is given by the ratio of V_{DS} to I_{DS} in its nonsaturated region of operation (the part of the I_D versus V_{DS} characteristics which radiate out from the origin). The JFET channel resistance can be used in a ratio with another fixed resistance to make an adjustable voltage divider. This creates a voltage-controlled attenuator, whose voltage division ratio is set by an externally applied voltage. Such an attenuator has the primary advantage of speed over a mechanical potentiometer, and it can also be put into feedback loops to provide automatic signal level control.

Set-Up

Construct the variable attenuator circuit as shown in Fig. E3.8 using the following components:

R1 = 4.7 kΩ 5% 1/4W resistor
R2, R3 = 100 kΩ 5% 1/4W resistor
J1 = MPF102 JFET

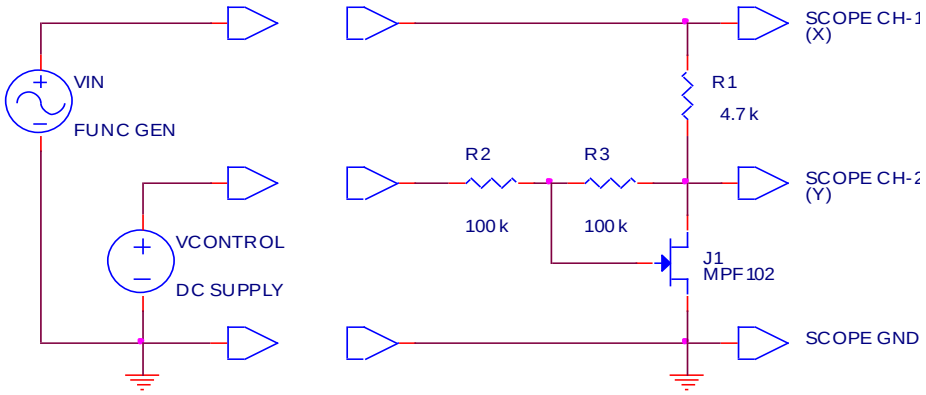

Figure E3.8

In this circuit, J1, R2, and R3 form an equivalent resistance in a voltage divider with R1. This particular connection of R2 and R3 is used to "linearize" the JFET's equivalent resistance, but they are sufficiently large in size to not affect the voltage division properties of the circuit. The function generator provides an input signal which needs to be attenuated, and the DC power supply provides a control voltage which sets the amount of attenuation.

Measurement-8

Configure the function generator to produce a 100 Hz, 1.0 V amplitude sine wave, and configure the DC power supply to produce an output control voltage of $V_{control} = -5.0$ V. Configure an oscilloscope to display the voltage transfer characteristic (VTC) of this circuit. Display the VTC on the

oscilloscope using 1 V/div on both the x and y axes. Sketch a copy of this VTC in your laboratory notebook, labeling both axes with tick marks and a voltage scale.

Next, examine the effect of the control voltage on the VTC of this voltage divider. Try to obtain the largest variation in the VTC that you can without forward biasing the JFET gate. Select two or three well chosen values for $V_{control}$ to demonstrate the variability of the VTC and sketch the corresponding VTCs on the same set of axes that you used for the first VTC.

Next, remove R3 and repeat the above on a new set of axes. You might also wish to view the distortion created by the nonlinear behavior of the JFET by using a triangular wave as the input signal from the function generator. Compare the output waveform shape to that which is applied to the input by the function generator. How does the amount of distortion vary with the amplitude of the input signal?

Question-8

(a) What range of attenuation (voltage division ratio) is produced by this circuit when R3 is present?
(b) What is the range of attenuation expressed in decibells (dB)?
(c) Show mathematically that the equivalent resistance of J1, R2, and R3 is $R_{equiv} = V_T^2/I_{DSS}*(V_{control} - 2V_T)$.
(d) Using the values of I_{DSS} and V_T that were obtained in Procedure 7 and the above expression for R_{equiv}, predict what the minimum and maximum equivalent resistances should be, and then what the minimum and maximum attenuation (voltage division ratio) of the circuit should be. Comment on how well the prediction matches to the experimental measurements.